Pango Design Suite User Manual

(2021.4 Version 3.1)

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1 About the manual

Pango Design Suite detailed manual is aimed at all Pango Design Suite users, aiming to help users quickly complete the FPGA design work through Pango Design Suite . The Pango Design Suite detailed manual provides detailed instructions on the basic operations, development process, and common errors of FPGA development using Pango Design Suite .

1.1 Software Introduction

Pango Design Suite is a tool software dedicated to FPGA development. Its main functions include design entry, synthesis, simulation, implementation and bitstream generation. Pango Design Suite has the characteristics of friendly interface and simple operation, and can complete the whole process development of FPGA with the help of some commonly used third-party EDA software (mainly logic synthesis tools and simulation tools) .

1.2 More help

Pango_Design_Suite_User_Guide
Pango_Design_Suite_Quick_Start_Tutorial
Pango_Power_Calculator_User_Guide
Pango_Power_Planner_User_Guide
Physical_Constraint_Editor_User_Guide
User_Constraint_Editor_User_Guide
Design_Editor_User_Guide
Fabric_Configuration_User_Guide
Fabric_Debugger_User_Guide
Fabric_Inserter_User_Guide
IP_Compiler_User_Guide
Simulation_User_Guide
ADS_Synthesis_User_Guide
ADS_Language_Support_Reference_Manual
Route Constraint Editor User Guide
Timing Analyzer User Guide
Pango SSN Analyzer User Guide
Pango SSN Estimator User Guide

2 Basic operation

The following are based on the introduction of the PGL50H line under the Logos series, and the default settings are generally used.

2.1 Start the software

Double-click the Pango Design Suite shortcut on the desktop or click the corresponding Pango Design Suite shortcut in the program menu to start Pango Design Suite . The initial interface of Pango Design Suite after startup is shown in the figure below:

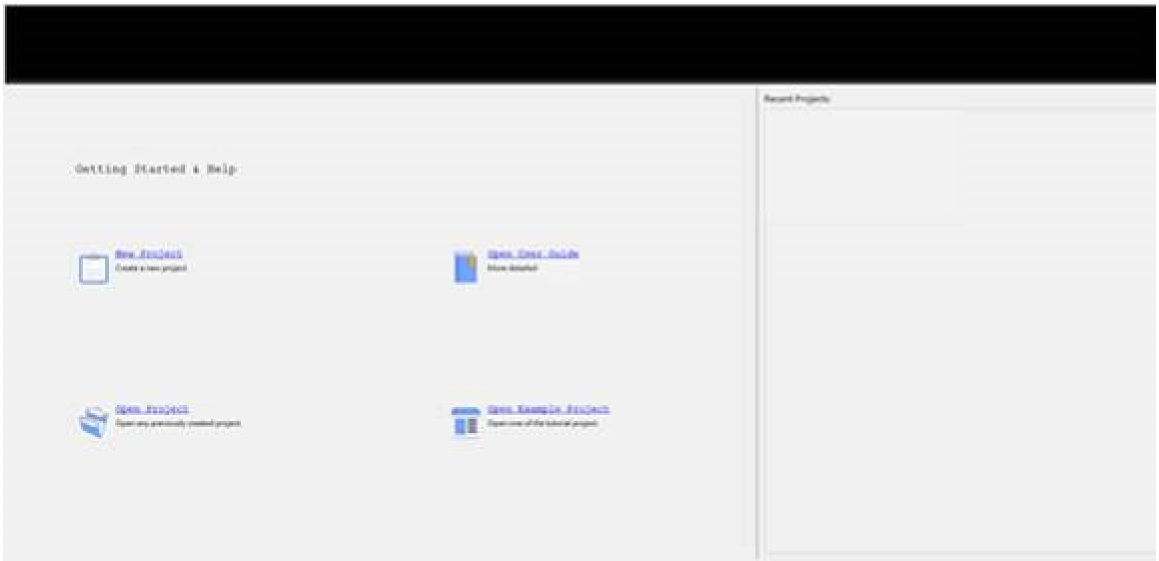


Figure 2 -1 Initial interface

Every time you start the software, if the software license is about to expire (less than or equal to 30 days), it will prompt the license expiration time. It can allow users to have enough time to plan and apply for a license in advance , so as not to delay the project progress.

2.2 New project creation

New construction can generally be carried out in two situations, one is to create a new project in the initial interface of the software startup; the other is to create a new project on an existing project. There are two ways to enter the initial interface of the software startup, the first is to start the software, and the other is to select the [Close Project] item of the Project menu in the existing project to close the current project and jump to get it.

(1) To create a new project is mainly to open the new project wizard [New Project], and then set it. By creating a new project in the initial interface of the software startup, there are three ways

to create a new project, which will be introduced below; when creating a new project on top of an existing project, you can choose the first two ways to create a project.

a . You can select the menu item 【 Project 】 / 【 New Project… 】 command. As shown below:

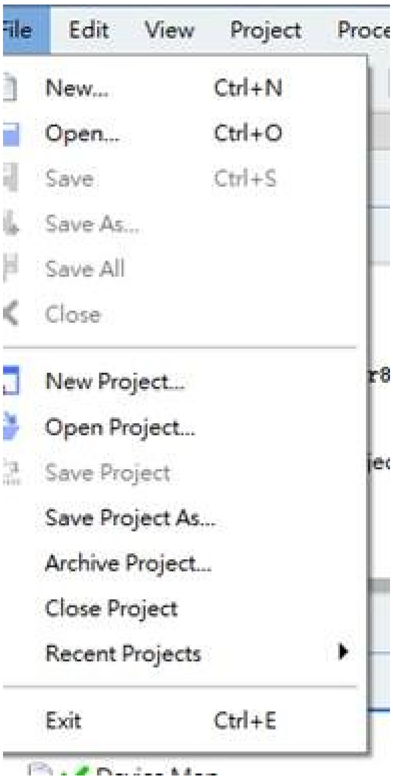


Figure 2 -2 New Project - Menu

b . Can be opened by the New Project shortcut command. As shown below:

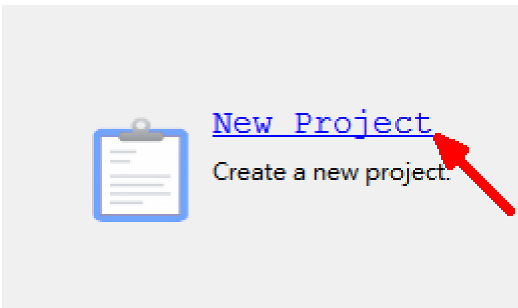


Figure 2 -3 New Project - Shortcut

(2), the new project wizard [New Project], as shown in the following figure:

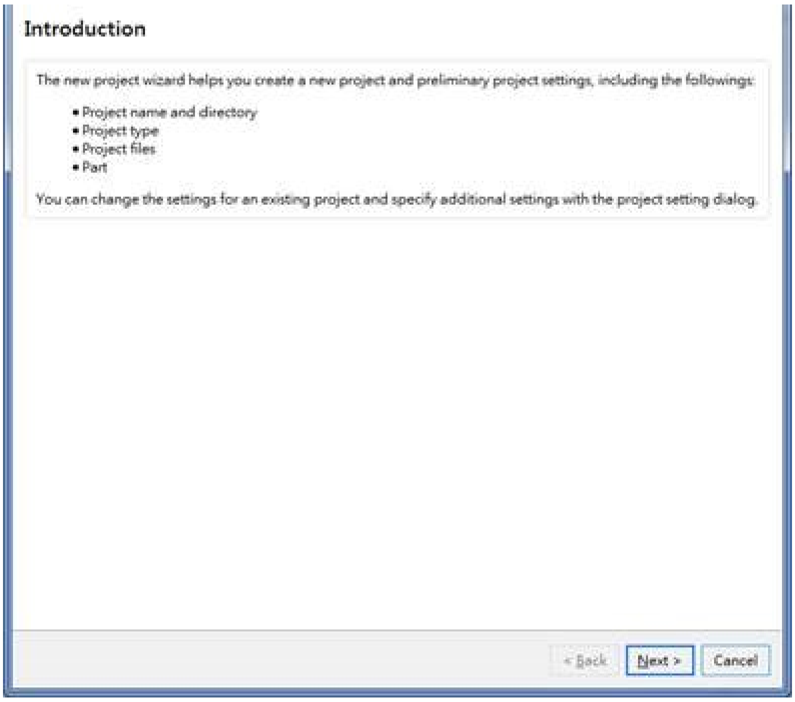


Figure 2-4 New project introduction page

Brief introduction of new construction. Creating a new project generally includes setting the project name and project path, project type, project file and device information. Click Next and the following interface appears:

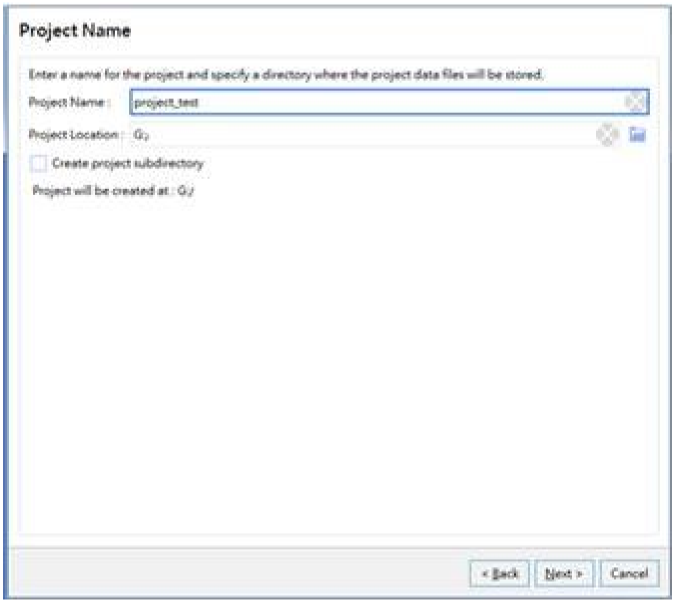


Figure 2-5 New Project Wizard

【 Project Name 】The default is **project** , which is the name of the project file. (Only letters, numbers, underscores (_), dashes (-), dots (.) are allowed). This example defaults to project . In particular, IPC filenames only allow letters, numbers and underscores (_).

[Project Location] is used to select the working path of the new project (the folder name only allows letters, numbers, underscores (_), bars (-), dots (.), @ , ~ , ,, + , = , # , spaces ( ), but

spaces cannot appear at the beginning and end of the path name), that is, the path where the project file is placed. For example, when you choose to add files, the dialog box for adding files in the software will use this path as the default path. In addition to supporting the operation mode of the project file mode, the software also supports the script mode, and the relative path in the script is relative to this path. For example , the tcl command add_design –verilog ./add.vm is in the working path by default. Under normal circumstances, files such as source files will be placed in this folder. This example selects G:/ .

【 Create Project Subdirectory 】 Use the project filename as part of the working directory.

After setting the project name and project path, click Next to display the interface for selecting the project type:

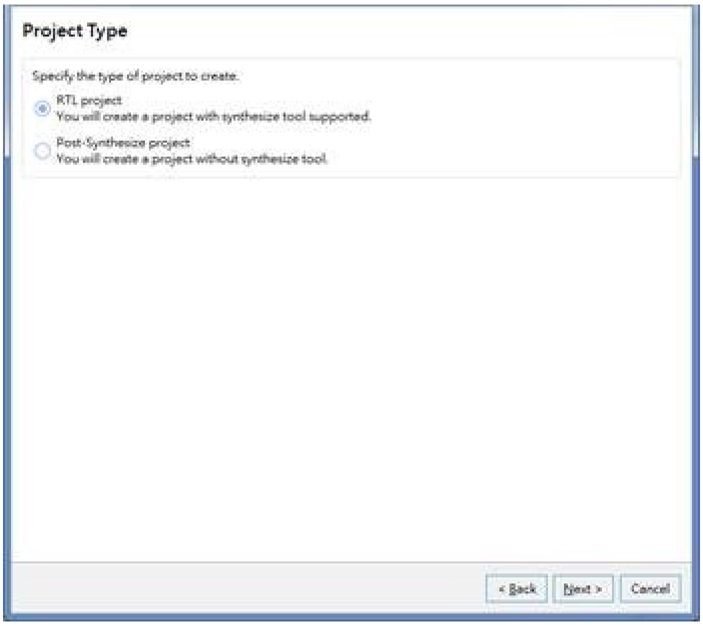


Figure 2-6 New project type interface

【 RTL Project 】 used to create RTL projects. The new project can execute synthesize , device map , place& route , report timing , report power , generate netlist and generate bitstream , etc.

【 Post-Synthesize Project 】 used to create post-synthesis projects. The new project can execute device map , place& route , report timing , report power , generate netlist and generate bitstream , etc.

After selecting the project type, click Next and the interface for adding rtl files will appear:

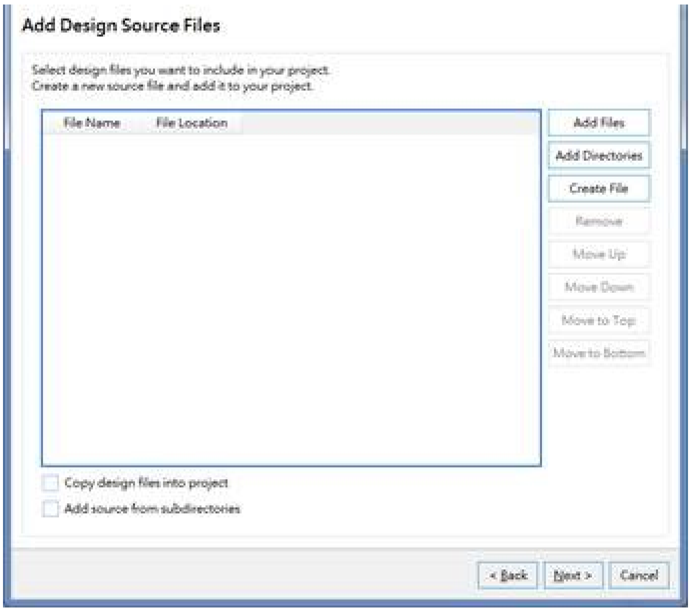


Figure 2-7 Add designs to new projects

This interface , Add Files and Add Directories can be used to add rtl source files and create new rtl source files, and adjust the compilation order of rtl files. Add Files adds the selected files, and Add Directories adds all appropriate files under the selected folder. If checked The Add source from subdirecotires below adds all the appropriate files in the subdirectory. After adding the rtl file, click Next to display the Add IP interface. The Add Files and Add Directories of the IP interface are the same as above:

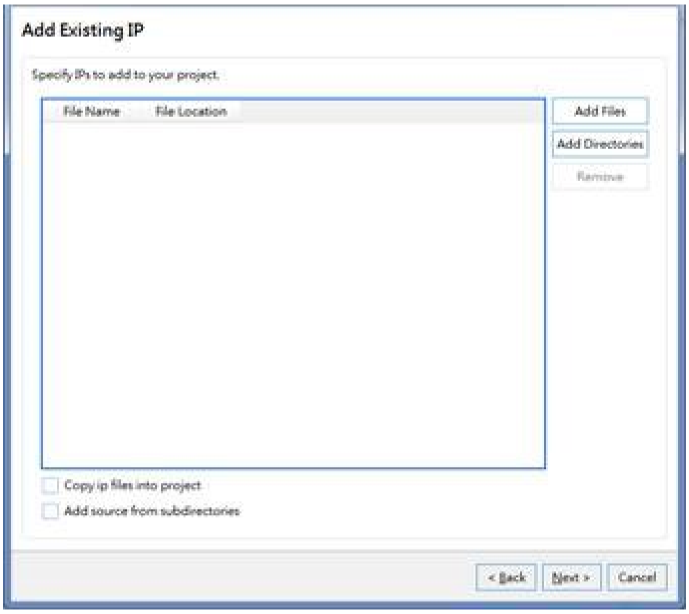


Figure 2-8 New project to add IP

This interface can add IP files. Click Next and the interface for adding constraints appears:

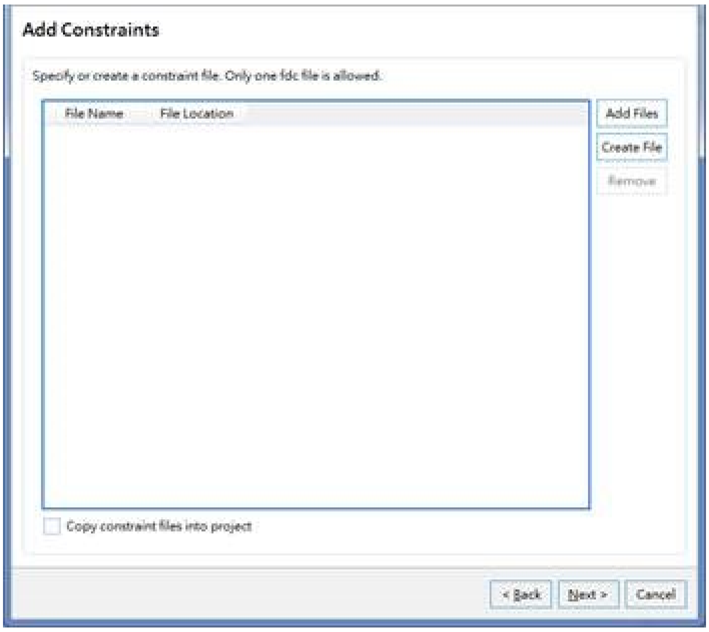


Figure 2-9 Add constraints to new projects

This interface can add or create constraint files. Click Next to display the device selection interface:

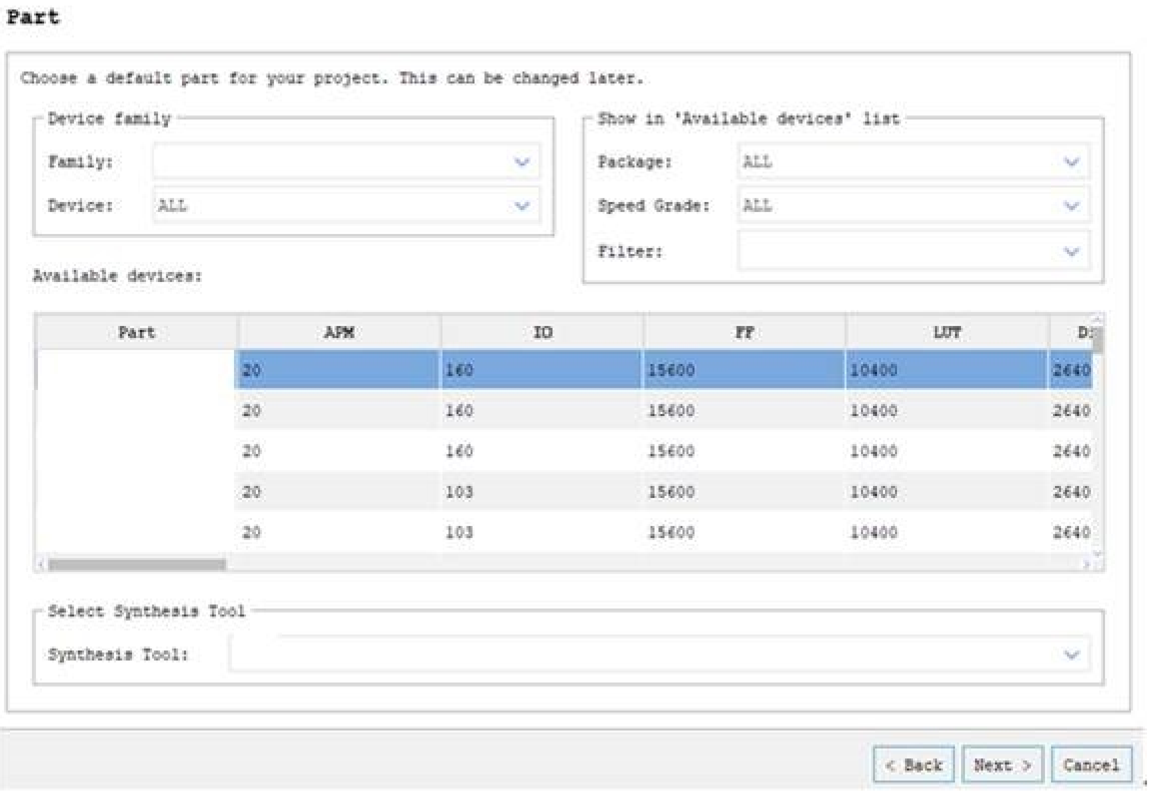


Figure 2-10 New project selection device

In this interface, you can select the required synthesis tool through the drop-down list of Synthesis Tool . The PDS with Synplify Pro tool can be configured with Synplify Pro and ADS .

PDS without Synplify Pro tool only has ADS as a synthesis tool. After configuring the comprehensive tool, click Next to display the summary interface:

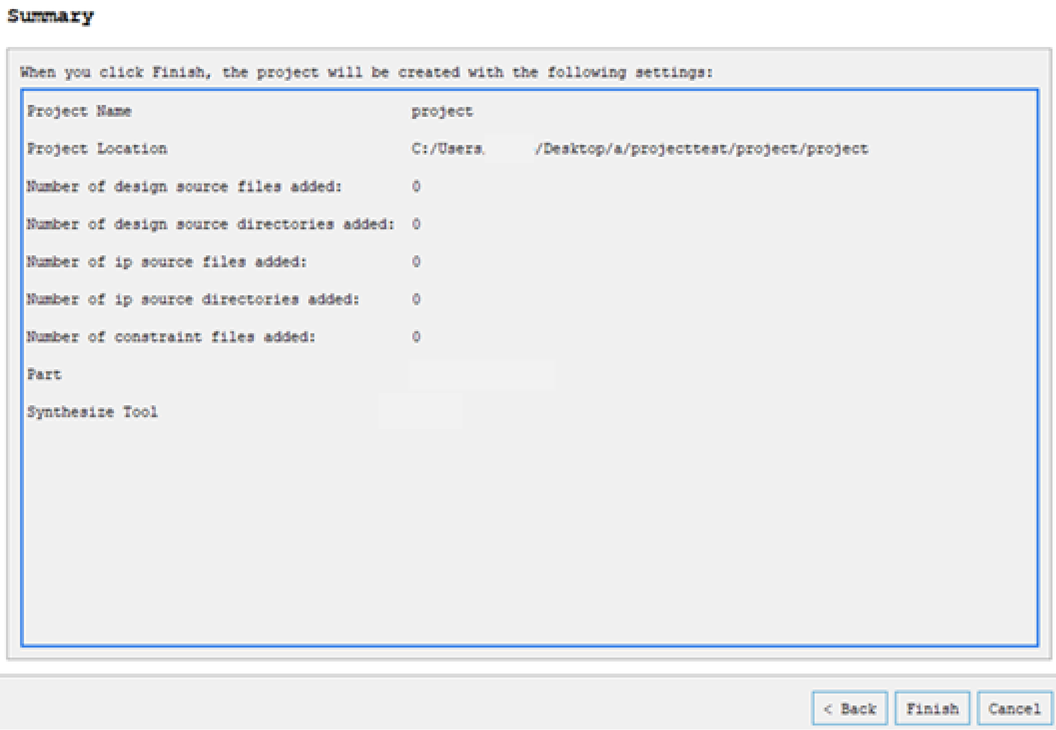


Figure 2-11 New project summary interface

(3), click the Finish button, the project is created. After the project is created, the software is shown in the figure below.

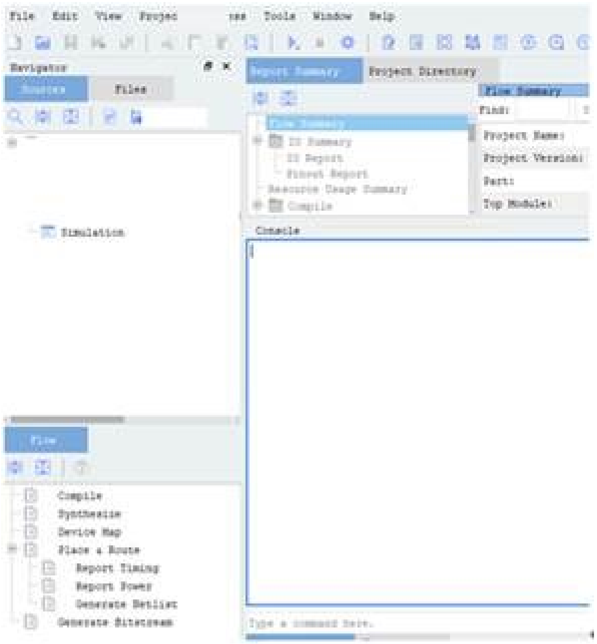


Figure 2-12 The main interface of Pango Design Suite after the project is established

2.3 Main interface

After creating a new project, the main interface of Pango Design Suite appears , as shown in the figure below, which is divided into seven parts from top to bottom: title bar, menu bar, tool bar, project management area, report area, console, and status bar.

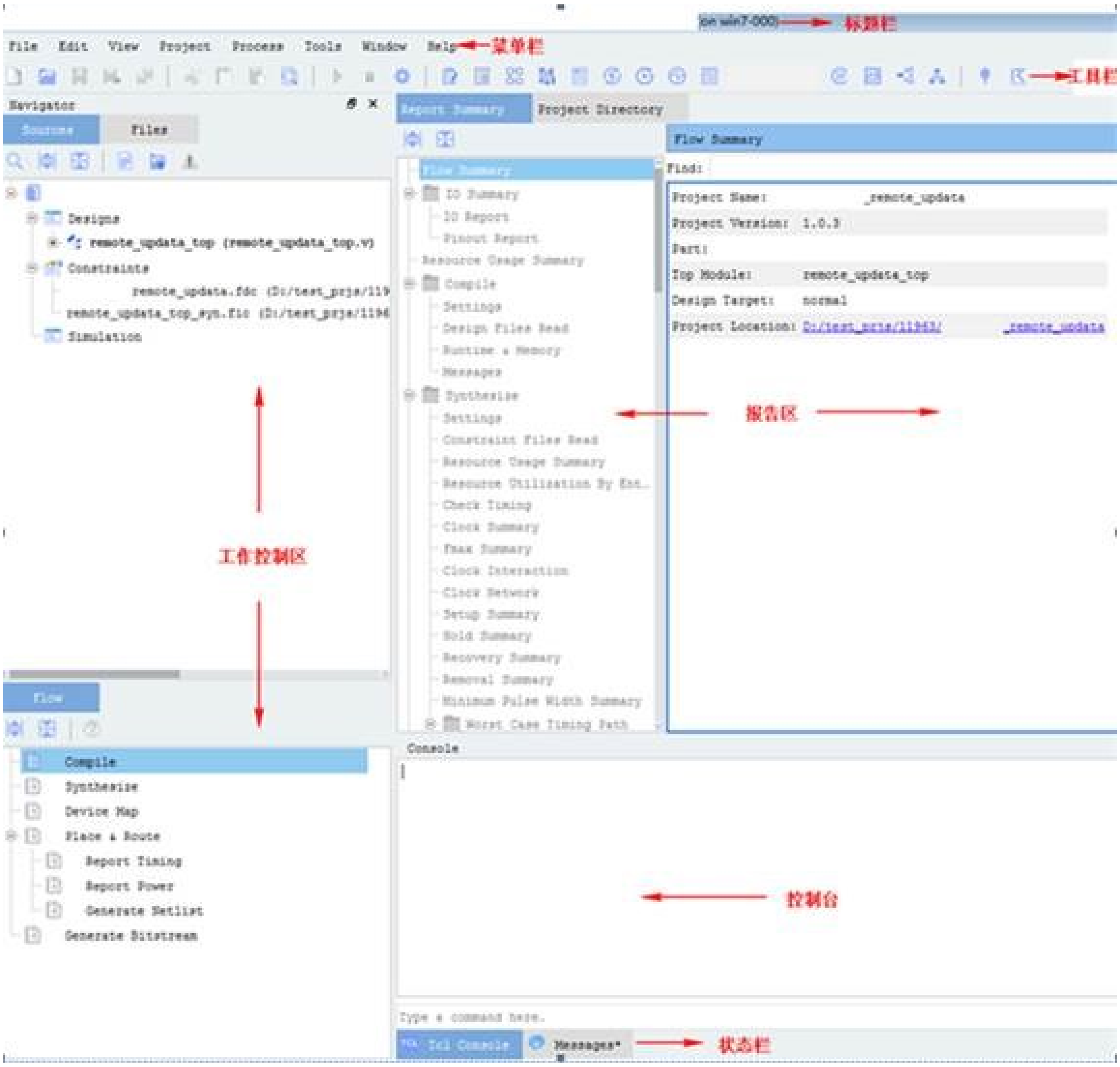


Figure 2-13 Main software interface

Title bar: mainly displays the name of the current project (including the project path).

Menu bar: mainly includes " File ", " Edit ", " View ", " Project ", " Process ", " Tools ", "Window" and "Help" 8 drop-down menus. Its use method is similar to common Windows software.

Toolbar: mainly contains shortcut buttons for frequently used commands. The shortcut buttons in the toolbar can be found in the menu bar, and the flexible use of the toolbar can greatly facilitate the user's operation in the software.

Project management area [Navigator]: This window is the main part of the software operation, and related operations are closely related to the FPGA design process, including basic functions such as design input, synthesis, design implementation, and configuration file generation. After an action, an icon appears in front of a processing step to indicate the status of the step. The project management area includes [Sources] and [Flow] two parts. 【 Sources 】 It is mainly used to select devices, add test vectors and constraint files, etc. 【 Flow 】 Related operations are closely related to the Fabric design process, including synthesis, Map , PnR , and configuration file generation.

Report area [Report Summary]: The report area is mainly to display some report information according to action classification during the software running process.

Console 【 Console 】 : Display software processing information, such as operation step information, warning information and error information, etc. The Tcl Console label at the lower left foot of the console can input tcl commands in this window to realize the command line operation and script operation of the software. Error , critical warning , warning , and info messages are displayed in a tree structure in another tab Messages window at the lower left of the console . The number of various messages is displayed at the top of the window , and the check boxes of errors , critical_warnings , warnings , and infos control whether this type of information needs to be displayed in the message box. The Message window supports the folding and unfolding of the information tree and the search function for each message . The Message window supports grouping by message ID , that is, the first message with the same ID is the parent node, and the rest are the child nodes of the parent node. The parent node needs to provide the number of its child nodes (messages).

Status bar: Displays related commands and operation information.

2.4 Menu introduction

Pango Design Suite can be completed through the menu, the main menu and corresponding functions are briefly introduced below.

(1) File menu

File menu commands include New..., Open..., Save, Save As..., Save All, Close, New Project..., Open Project... , Save Project , Save Project As... , Archive Project... , Close Project , Recent Projects , and Exit .

File menu is shown below:

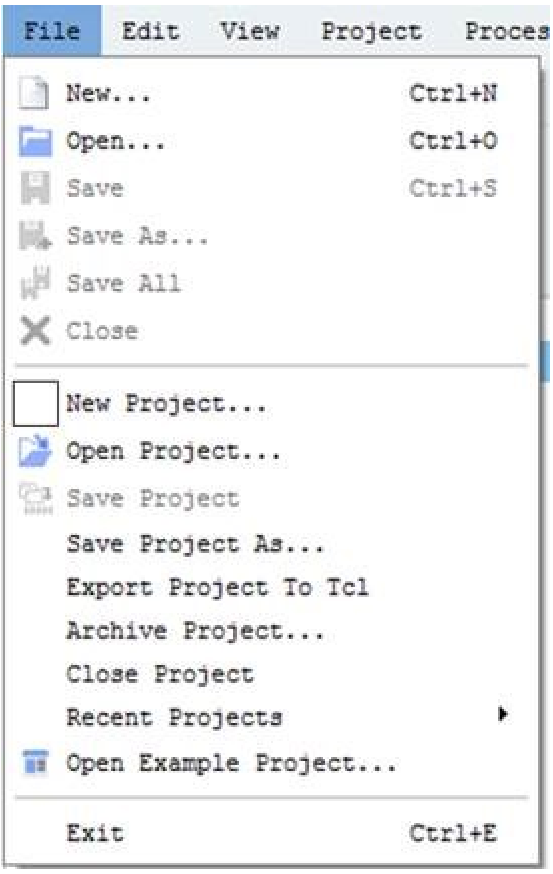


Figure 2-14 File menu

【 New… 】 : used to create a new source file, the shortcut key is " Ctrl+N ".

【 Open… 】 : used to open files in the file formats supported by Pango Design Suite software.

【 Save 】 : Used to save the current source file.

【 Save As… 】 : It is used to save the current source file.

【 Save All 】 : Used to save all currently opened source files.

【 Close 】 : Close the current file.

【 New Project... 】: create a new project

【 Open Project... 】: used to open an existing Pango Design Suite project

【 Save Project 】: Save the current project

【 Save Project As… 】: Save the current project as

【 Export Project To Tcl 】: Export the current project as a Tcl script file

【 Archive Project … 】: Pack the current project into a compressed package

【 Close Project 】: Close the current project

【 Recent Projects 】: Open the list of recently operated project files

【 Exit 】: Exit the software, the shortcut key is "Ctrl+E" .

Among them , after Export Project To Tcl is opened, the interface is as follows:

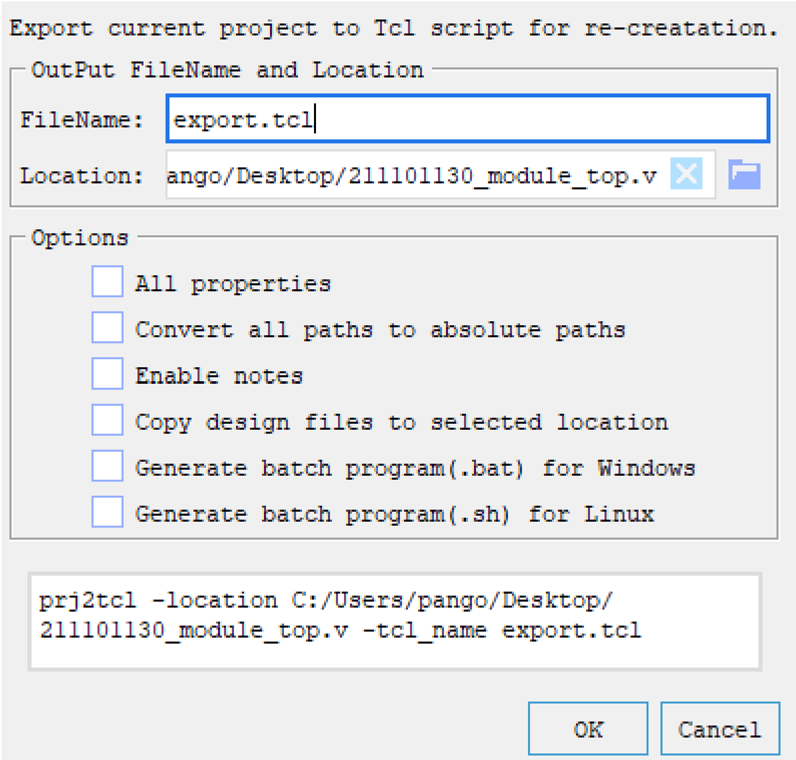


Figure 2-15 Export project to tcl

【 FileName 】: Specify the file name of the exported tcl file.

【 Location 】: Specify the path to export the tcl file.

【 All properties 】: After checking this item, all options are checked.

【 Convert all paths to absolute paths 】: Convert the relative paths in the file to absolute paths.

【 Enable note 】: Comment on the usage of Tcl command.

【 copy design files to selected location 】: Copy the Design files in the file to the selected path.

【 Generate batch program(.bat) for windows 】: Generate a Bat file to quickly open PDS and run tcl script on Windows platform .

【 Generate batch program(.sh) for Linux 】: Generate a Sh file to quickly open PDS and run tcl script on the Linux platform .

After the operation is completed, the corresponding prj2tcl command can be generated in the command bar, and then click OK , and the tcl file can be generated in the specified path . You can also execute the generated prj2tcl command in the tcl console to export the tcl file.

(2) Edit menu

Edit menu include Cut , Copy , Paste , and Preferences... .

Edit menu is shown below:

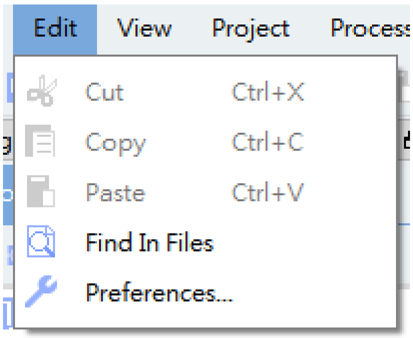


Figure 2-16 Edit menu

【 Cut 】: Cut and paste the selected code, the shortcut key is "Ctrl+X" .

【 Copy 】: Copy the selected code, the shortcut key is "Ctrl+C" .

【 Paste 】: Paste the cut and copied code, the shortcut key is "Ctrl+V" .

【 Find In Files 】: Query and search the input keywords in the files.

【 Preferences... 】: Configuration options , as shown below. Set Pango Design Suite text style, integrated tool path, License settings.

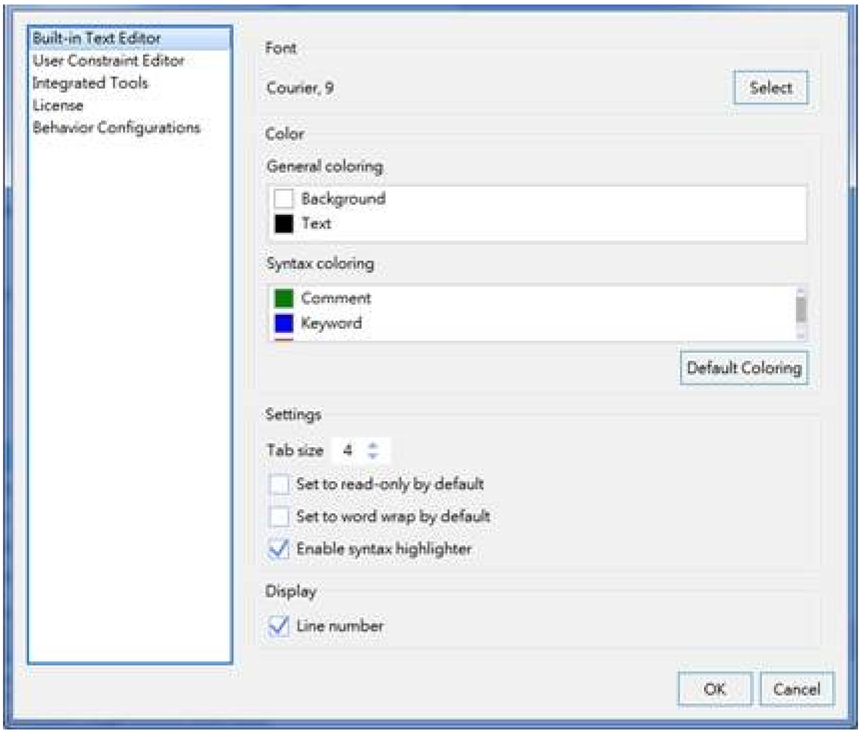


Figure 2-17 Preferences settings

Click User Constraint Editor to display the configuration UCE interface. This interface can be configured to analyze the entire netlist or only the top-level port when entering UCE , as follows:

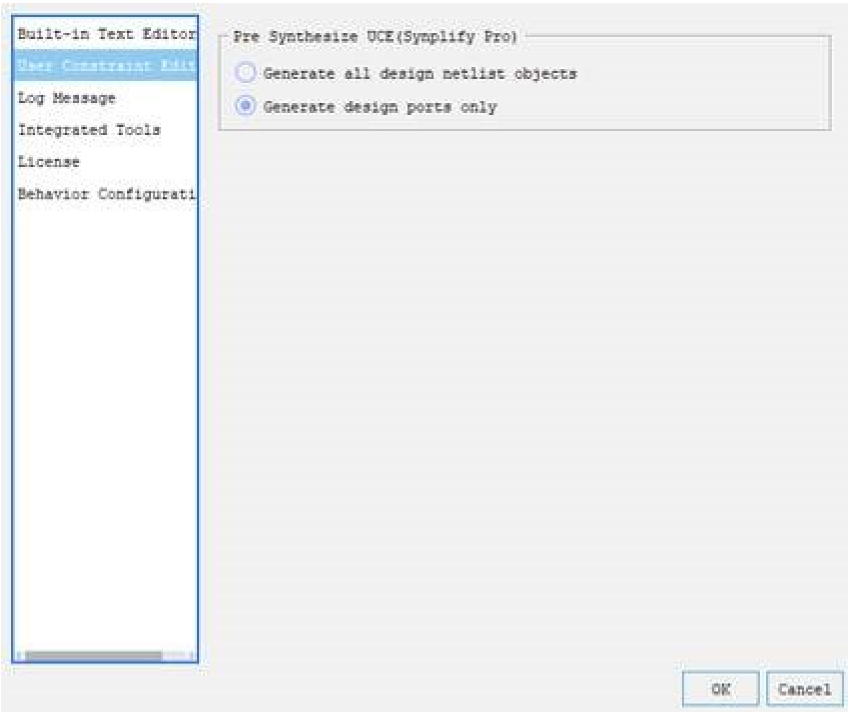


Figure 2-18 UCE netlist analysis configuration

Click **Integrated Tools** to edit the path of **Synplify Pro** (only the PDS with Synplify Pro tool has this setting item) and the path of the third-party text editor, as shown in the figure below:

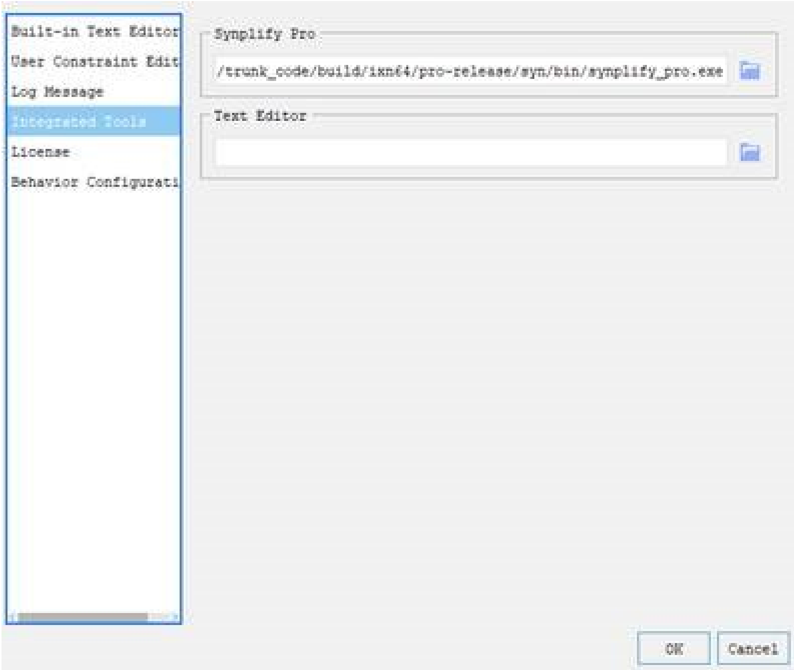


Figure 2-19 Integrated Tools configuration

In the figure above, click license and the following interface will appear:



Figure 2-20 License setting

Among them , PANGO_LICENSE_FILE is used to set PDS , and SNPSLMD_LICENSE_FILE is used to set Synplify license (only PDS configured with Synplify Pro tool has this setting item). These two settings have the same effect as those set in the system environment variables.

Click Behavior configuration to display the humanized anti-misoperation configuration interface, with the following configurations:

Ask before run out-of-date implementation : whether to prompt when run out-of-date appears

Ask before rerun implementation : Click the rerun button to configure prompts

Ask before rerun all implementation : Whether to configure prompts when clicking the rerun all button

Ask before close project : Whether to configure the prompt function when closing the project

Ask before close PDS : Whether to configure the prompt function when closing the software

Open recent project before starting PDS : Whether to open the recent project when starting PDS

The interface that appears is as follows:

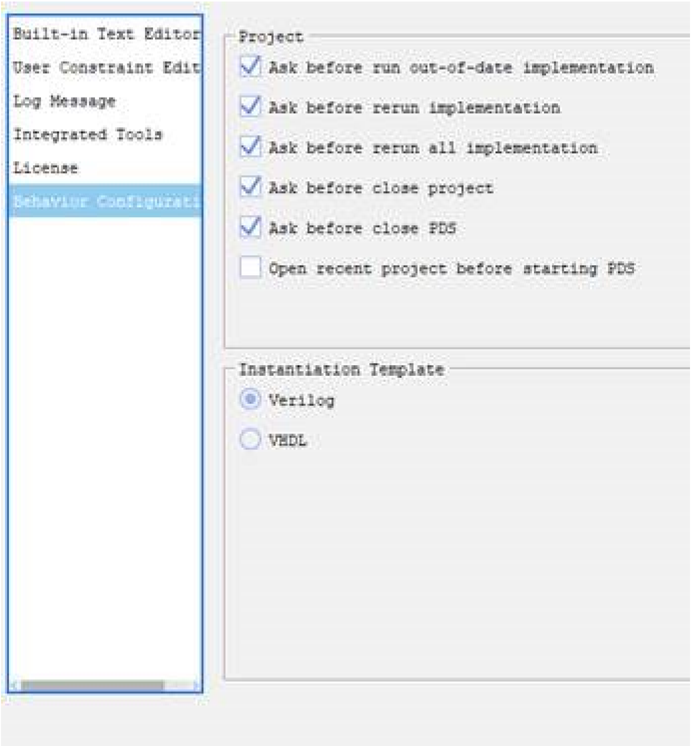


Figure 2-21 User-friendly misoperation configuration

Instantiation Template is the language format of the instance template generated by user configuration.

(3) View menu

View menu include Reset Window Layout , Navigator , Console , File Tool , Edit Tool , Process Tool , Widget Tool , and Help Tool . The functions of the commands can be seen from the names. If you check the relevant options, there will be corresponding graphics displayed on the software interface.

View menu is shown in the figure below:

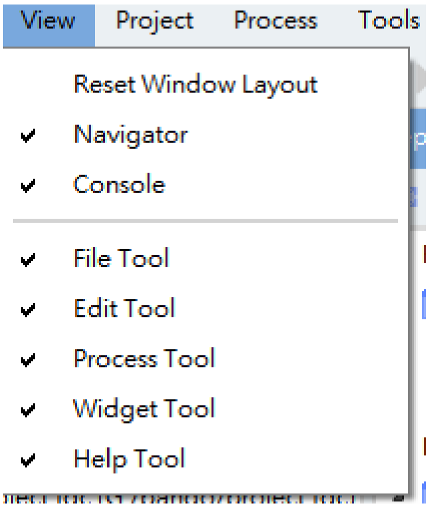


Figure 2-22 View Menu

(4) Project menu

Project menu include New IP , Add Source , and Project Setting .

Project menu as shown below

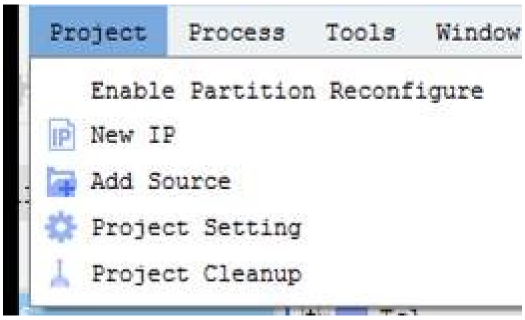


Figure 2-23 Project menu

【 Enable Partition Reconfigure 】: Partial dynamic reconfiguration

【 New IP 】: Create a new IP to the current project.

【 Add Source 】: Add a new source file for the current project.

【 Project Setting 】: Set current project options

【 Project Cleanup 】: You can selectively clean up the temporary files generated by the project running process.

(5) Process menu

Process menu include Run , Rerun , Rerun All , Stop , Run Simulation , and Pre Synthesize Constraint Check . Process menu as shown below

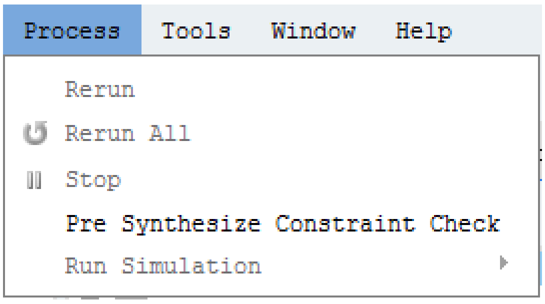


Figure 2-24 Process menu

【 Rerun 】: Re-execute all unexecuted operations before the currently selected operation (including the previously selected operation). If the operation before the currently selected operation is out of date , skip this operation.

【 Rerun All 】: Re-execute all operations of the current operation and its previous steps.

【 Stop 】: Immediately stop the current operation.

【 Run Simulation 】: Run simulation.

【 Pre Synthesize Constraint Check 】: Constraint check. The function of this button is to check all constraint files added to the project (excluding lcf and scf constraint files). If you need to check a single constraint file, right-click the constraint file in the project to check a single constraint file. The ADS process uses this function to generate a constraint inspection report (.ccr) , and the OEM process uses this function to generate a constraint inspection report (.rpt) .

(6) Tools menu

Tools menu include User Constraint Editor (Timing and Logic), Physical Constraint Editor (Post-Map), Route Constraint Editor , Design Editor , Power Calculator , Power Planner , Timing Analyzer , Inserter , Debugger , Configuration , IP Compiler , Synplify Pro , Compile Simulation Libraries , Schematic Viewer (View RTL Schematic , View Technology schematic).

Tools menu is shown in the figure below

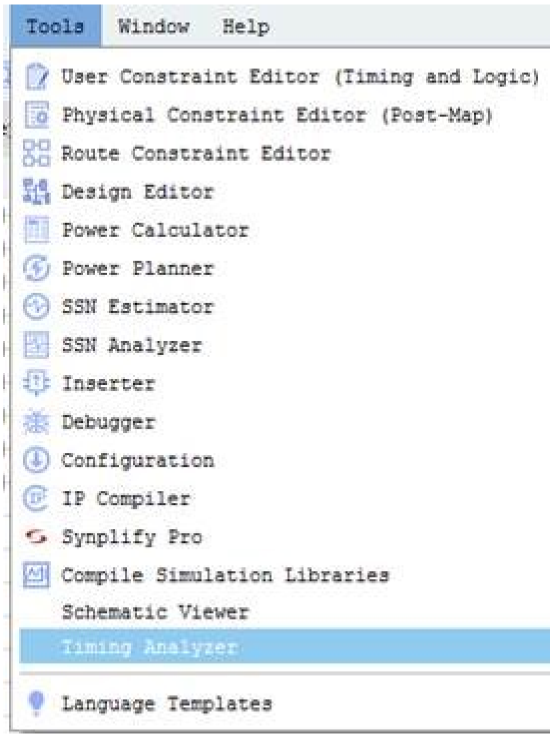


Figure 2-25 Tools menu

【 User Constraint Editor (Timing and Logic) 】: user constraints

【 Physical Constraint Editor (Post-Map) 】: Open physical constraints

【 Route Constraint Editor 】: Open routing constraints

【 Design Editor 】: View PnR results or perform manual PnR

【 Power Calculator 】: power consumption analysis software

【 Power Planner 】: power consumption estimation software

【 Timing Analyzer 】: timing analysis tool

【 SSN Estimator 】: Synchronous noise estimation tool

【 SSN Analyzer 】: Synchronous noise analysis tool

【 Inserter 】: Inserter software

【 Debugger 】: Debugger software

【 Configuration 】 : Configuration software

【 IP Compiler 】: IP Compiler software

【 Synplify Pro 】: Synplify Pro software (only PDS with Synplify Pro tool has this item)

【 Schematic Viewer 】: Contains the following two menu items

【 Compile Simulation Libraries 】: Compile simulation library

【 View RTL Schematic 】: Open RTL Schematic Viewer

【 View Technology Schematic 】: Open Technology Schematic Viewer

【 Language Templates 】: commonly used template information, the following chapters have specific introductions

(7) Window menu

Window menu is shown in the figure below

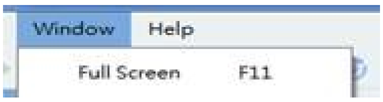


Figure 2-26 Window menu

Window menu is used to control whether the software is displayed in full screen (Full Screen).

(8), Help menu

Help menu commands include Help Topics , Software Manuals , and About . Help menu as shown below

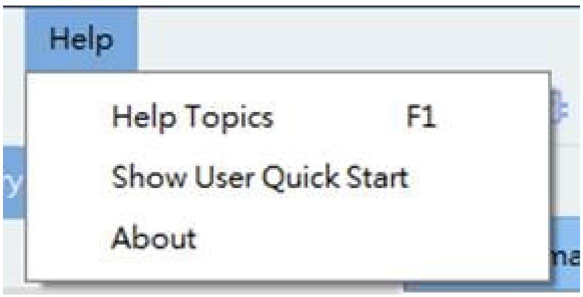


Figure 2 -27 Help menu

【 Help Topics 】: Display Help assistant.

【 Show User Quick Start 】: View the Pango Design Suite user manual.

【 About 】: Display Pango Design Suite About information.

2.5 Tool introduction

The toolbar is a shortcut to the commonly used menu bar. Right-clicking the toolbar can directly call up the View menu. The following introduces Language Templates , Report Summary and Run . For others, please refer to the introduction of the menu bar.

(1) Language Templates

Language Templates can quickly find some commonly used primitives, tcl commands, GTP templates, constraint templates and other information, and can also implement definition editing operations. The editing interface supports CTRL+C copy operations, as shown in the following figure:

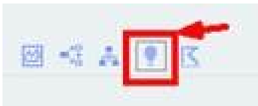


Figure 2 -28 Language Templates interface

(2) Report Summary

At present , the size of the PDS window is limited. When there are too many files opened, you need to move the tabs one by one to display the report summary , which is not very convenient. Therefore, add a shortcut to the report summary , as shown in the figure 2 -29 :



Figure 2 -29 Report Summary interface

(3) Run

Click the Run button in the menu bar to pop up the menu bar, and you can choose to perform different operations. If the process has been executed, the process will be re-executed, as shown in the figure 2 -30 :

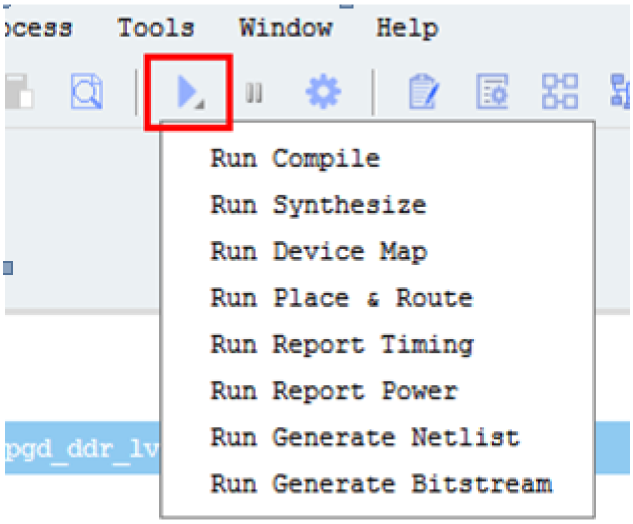


Figure 2 -30 RunTools

2.6 Open project

Opening a project can generally be carried out in two situations, one is to open an existing project in the initial interface of the software startup; the other is to open a project on an existing project. There are two ways to enter the initial interface of the software startup, the first is to start the software, and the other is to select the [Close Project] item of the Project menu on the current project page and close the current project.

(1) To open a project is mainly to open the project selection dialog [Open Project], and then select an existing project file. There are two ways to open a project in an existing project provider, as shown in a and b :

a . Open by selecting the menu item [Project] / [Open Project…]. As shown below:

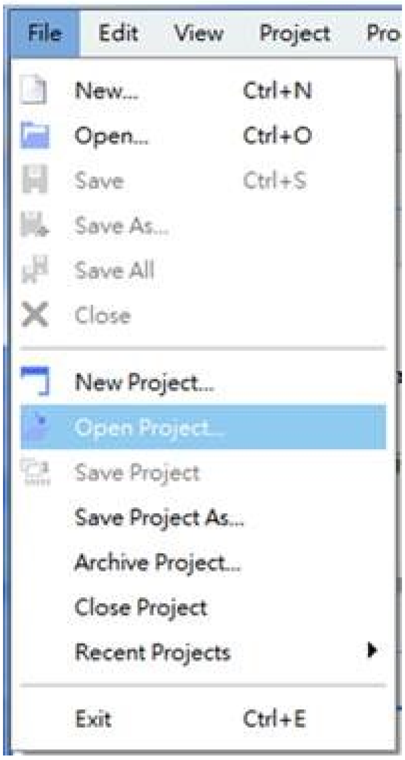


Figure 2 -31 Open the project - menu

b . Open via the Open Project shortcut command. Open the project - shortcut as shown below:

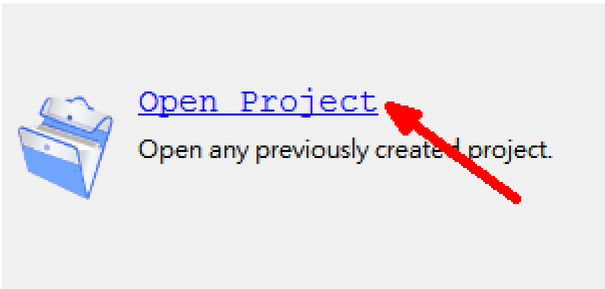


Figure 2 -32 Open project - shortcut

(2), open the project dialog [Open Project]. As shown below:

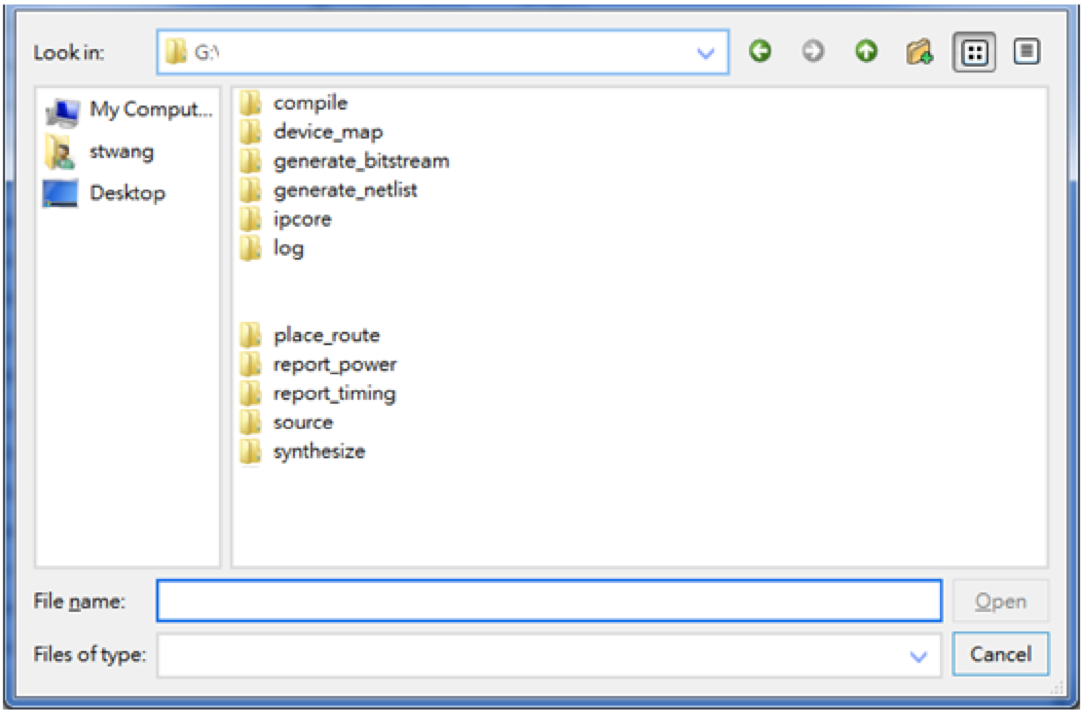


Figure 2-33 Open the project dialog

(3), select Finish After the .pds or .prj project file, click [Open] button to complete the operation of opening the project. After the project is opened, the software is as shown in the figure below.

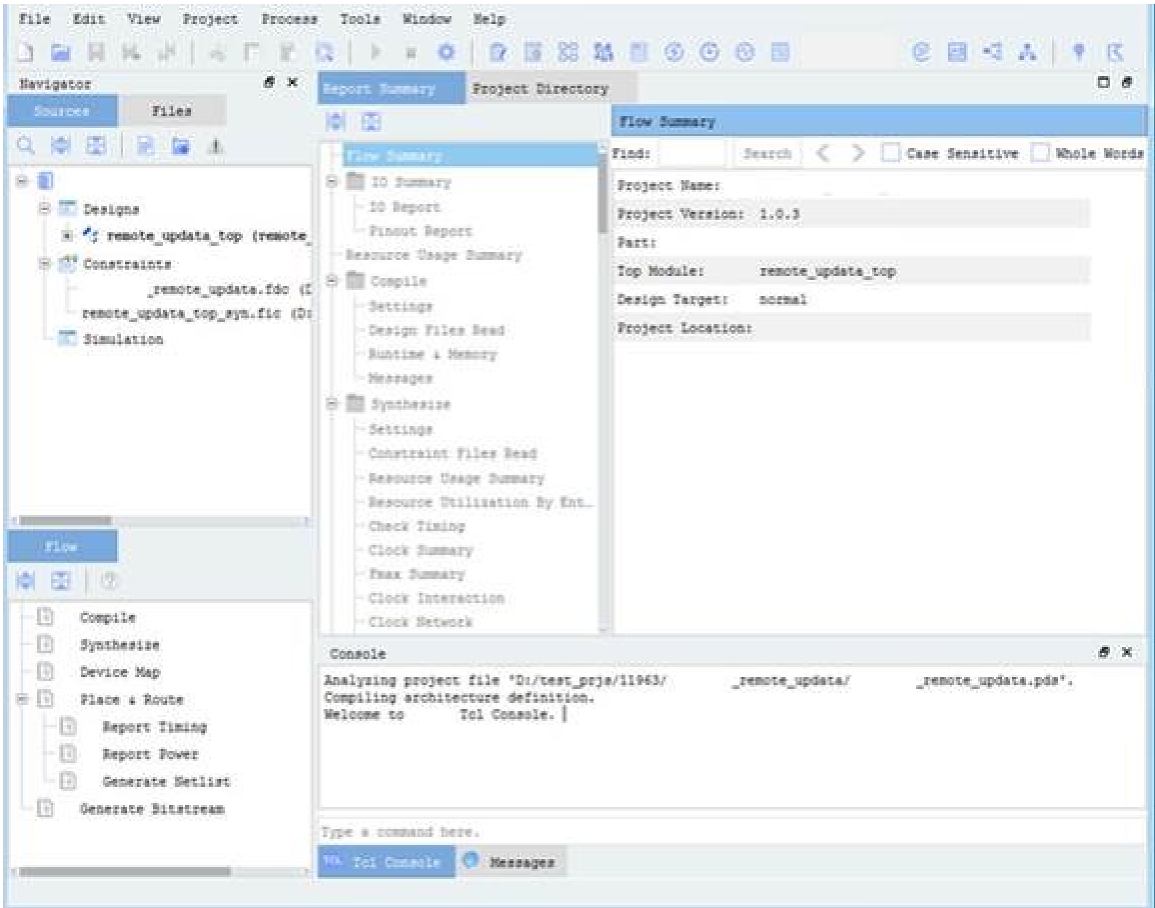


Figure 2-34 The main interface of Pango Design Suite after opening the project

In particular, for projects in the [Recent Projects] list, there are two ways to open them, mainly through the Recent Projects list. The following examples illustrate two ways to open project files in the Recent Projects list (up to ten projects):

a . It can be opened by selecting the project list under the menu item [Project] / [Recent Projects]. As shown in the figure below, open the Project - Recent Project - menu:

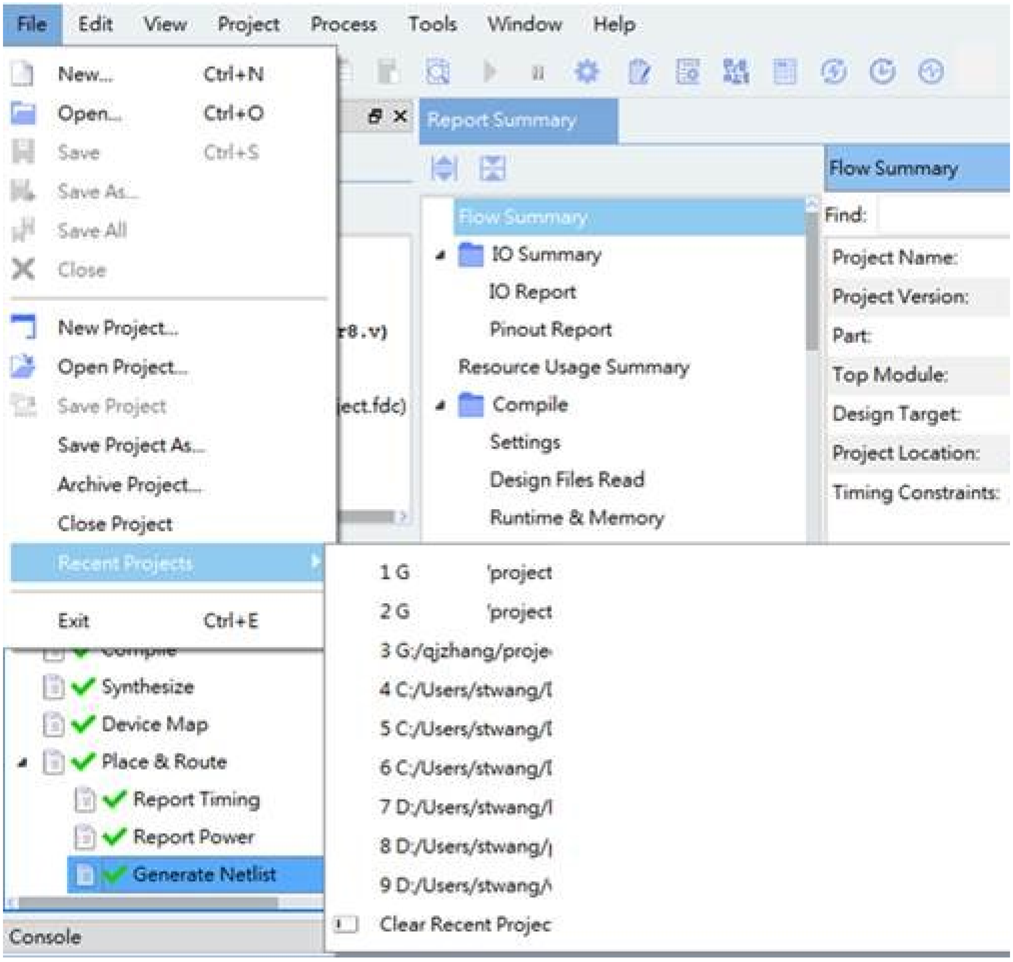


Figure 2 -35 Open Project - Recent Projects - Menu

When the mouse stays on a project menu item, the full path of the project will be displayed in the status bar below the PDS main interface;

b . In the initial interface of the software, it can be opened through the list of Recent Projects . As shown below:

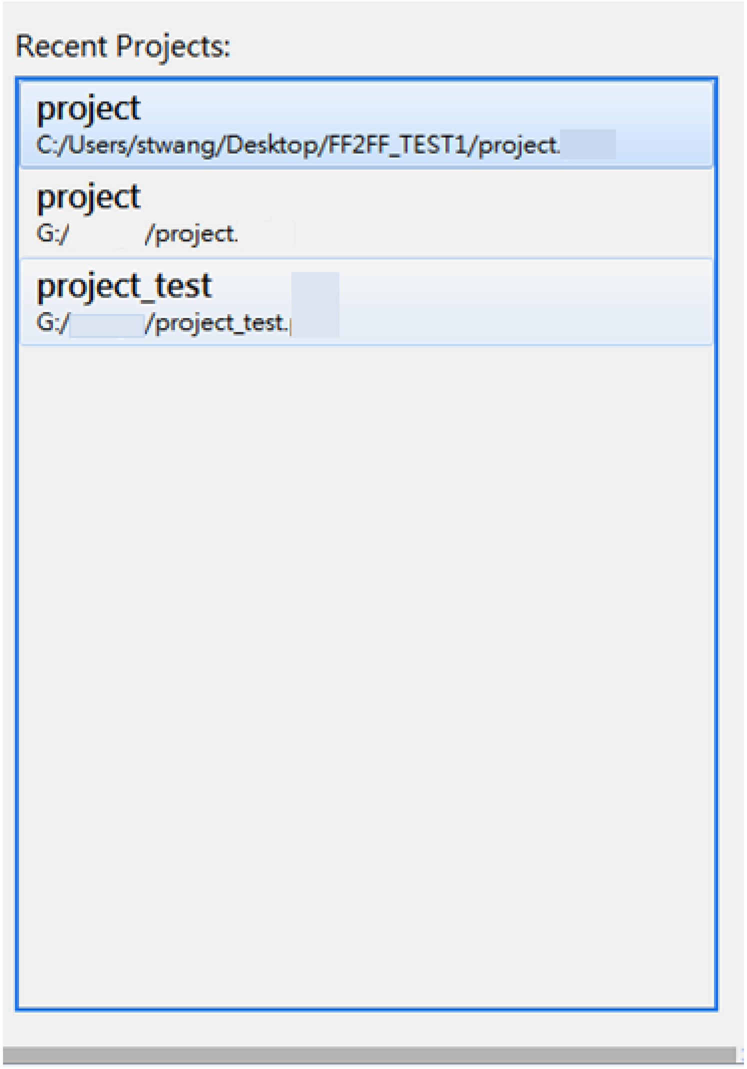


Figure 2 -36 Open project - recent project - wizard bar

If device information recorded in the opened project file does not exist, a prompt window for reselecting the device will pop up, as shown in the figure below:

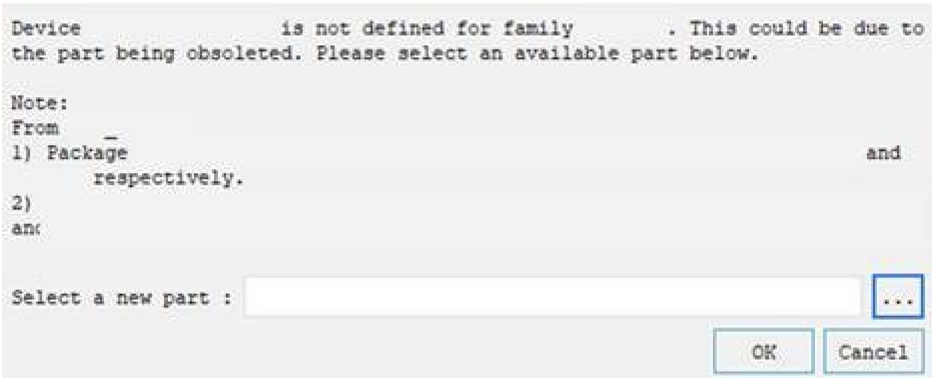


Figure 2 -37 Device information does not exist prompt window

The software will automatically fill in a device, click the " ... " button on the right to adjust the specific information, as shown in the figure below:

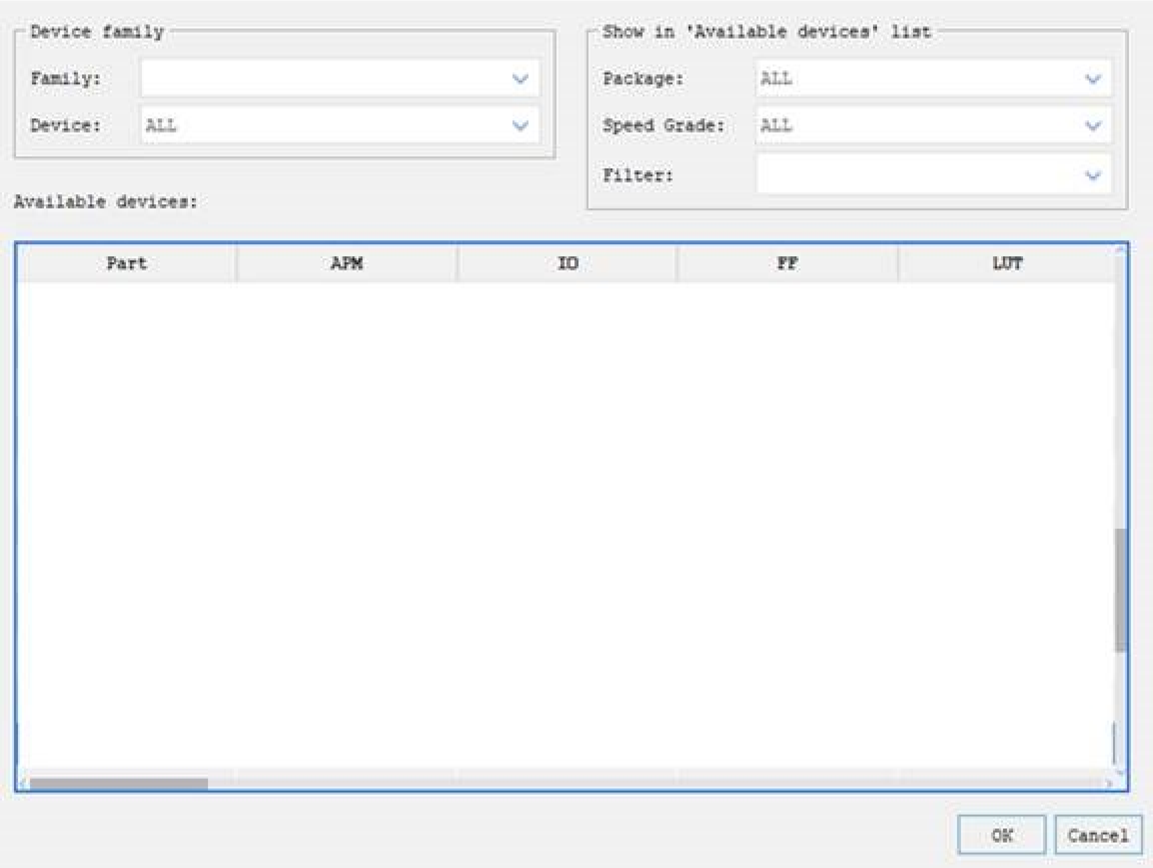


Figure 2-38 Select device information window

After selecting the device, click OK to open the project with the newly selected device, click cancel to return to the initial interface without opening the project.

2.7 Engineering Management

Navigator project management area is responsible for executing the workflow of the software and adding related files. You can double-click the left mouse button on the name of the work operation process to run it.

Navigator project management area is shown in the figure below

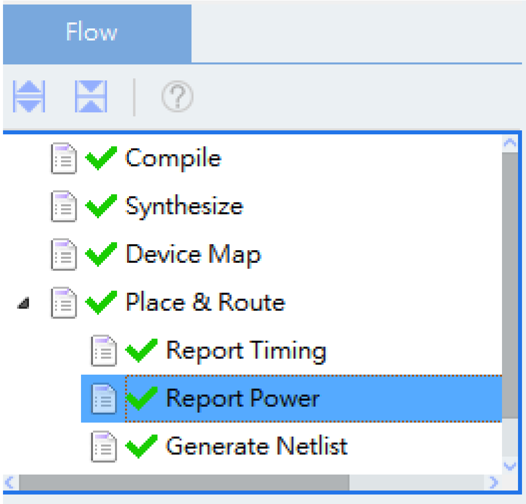


Figure 2 -39 Navigator Engineering Management Area

Navigator project management area can be divided into three parts : Sources , Files and Flow .

1 . The tasks or executives under Sources are introduced as follows:

【Device Information】: Double-click this column to pop up a box to select the device;

【 Designs 】: Choose to add Verilog or VHDL files in two formats;

【 Constraints 】: Add logical constraint files (timing constraints, etc.).

【 Simulation 】: Select to add test bench file

The right-click menu of the Source window is introduced as follows:

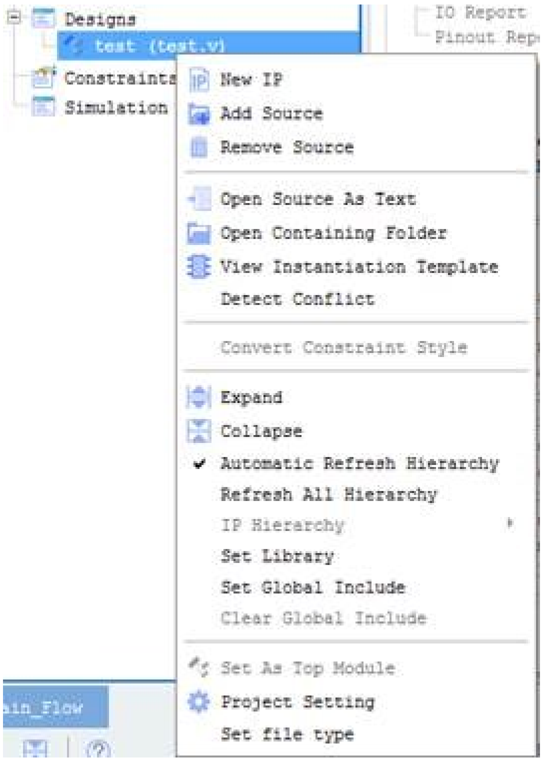


Figure 2-40 source window right-click menu

1) New IP : create a new IP

2) Add Source : Add hdl , constraints and other source files

3) Remove Source : remove the selected source file

4) Open Source As Text : Open the source file as text

5) Open Containing Folder : Open the folder where the source file is located

6) View Instantiation Template : instantiate design source , IP , module in simulation

7) Detect Conflict : Detect whether there is a scene where the ip idf file and the ip rtl file are added to the project at the same time

8) Convert Constraint style: Perform constraint conversion on the target file

9) Expand : Expand the current node

10) Collapse : Collapse the current node

11) Automatic Refresh Hierarchy : Automatically refresh the design hierarchy

12) Refresh Hierarchy : Manually refresh the design hierarchy

13) IP Hierarchy : Control whether to display the hierarchical structure of IP

14) Set Library : Set the library name for the target file

15) Set Global Include: Define the target file as a global include

16) Clear Global Include: Clear the target file from the global include

17) Set As Top Module: Set the current module as the top module

18) Project setting : project settings

19) Set file type : Set the file type

Among them, Set file type can set multiple file types, as follows:

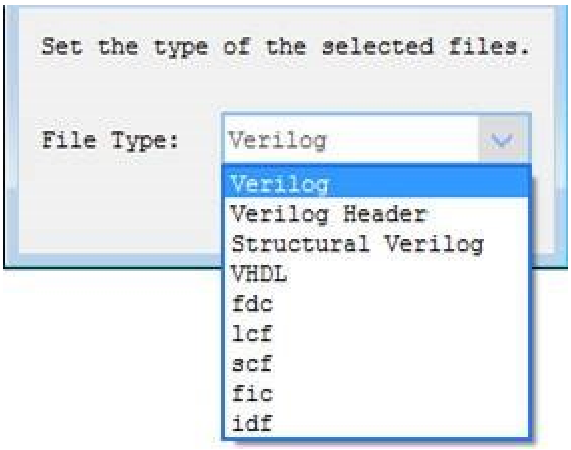


Figure 2-41 Set file type interface

Toolbar in the Sources area is introduced from left to right as follows:



Figure 2-42 File window toolbar

Search function: search by file name or module name

Expansion function: expand all the hierarchical structure of the source interface

Folding function: fold all the hierarchical structure of the source interface

New IP function: create a new IP

Add source function: add various types of source files

Missing file function: display modules that are not defined

3 . The content below Files is introduced as follows:

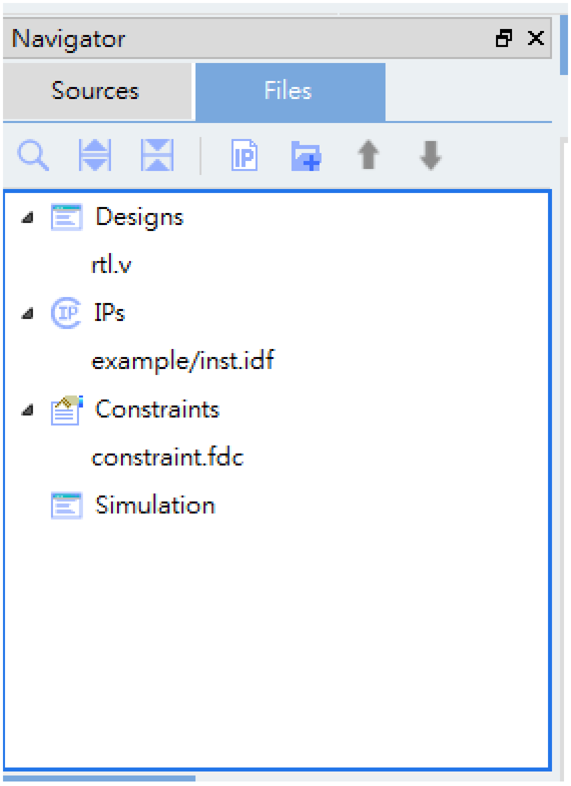


Figure 2-43 Navigator Engineering Management Area

【 Designs 】 : Choose to add Verilog or VHDL files in two formats;

【 Constraints 】 : Add logical constraint files (timing constraints, etc.).

【 Simulation 】 : Select to add test bench file

File window has exactly the same function as the toolbar of the Source window except for the latter two to set the compile order .

The right-click menu of the File window is introduced as follows:

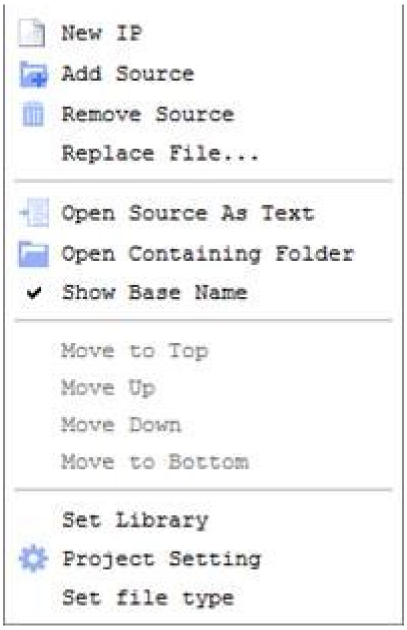


Figure 2-44 File right-click menu

1) IP : create a new IP

2) Add Source : Add hdl , constraints and other source files

3) Remove Source : remove the selected source file

4) Replace File… : replace the source file

5) Open Source As Text : Open the source file as text

6) Open Containing Folder : Open the folder where the source file is located

7) Show Base Name : Only display the file name, if unchecked, the file path will be displayed

8) Move to Top : Move the hdl file to the top of all source files

9) Move Up : Move the hdl file up

10) Move Down: Move the hdl file down

11) Move to Bottom : Move the hdl file to the bottom of all source files

12) Set Library : Set the library name for the target file

13) Project Setting : project settings

4 . The tasks or executives under Flow are introduced as follows:

【 Compile 】 : generate source code RTL netlist;

【 Synthesize 】 : synthesis;

【 Device Map 】 : Mapping, transforming design netlist files and mapping with device resources;

【 Place & Route 】 : layout and routing;

[Place & Route] / [Report Timing] Generate a timing report after placement and routing;

【 Place & Route 】 / 【 Report Power 】 Generate power consumption report after layout and routing;

[Place & Route] / [Generate Netlist] Generate a simulation report after layout and routing;

【 Generate Bitstream 】 : Generate a bitstream file.

Right-click menu in the project management area: Run , Rerun , Rerun All , Stop , Project Setting , Select a Seed To Apply in the right-click menu have the same functions as the corresponding part of the Process menu. As shown in the figure below, the Navigator right-click menu.

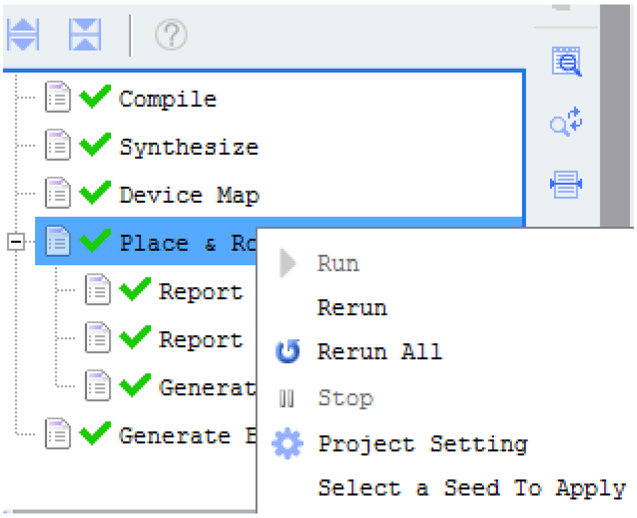


Figure 2-45 Navigator right-click menu

In the project management area, you can double-click with the left mouse button to perform an operation, or select each function, and then right-click to select the [Run] or [Rerun] command to perform this operation. You can also select the [Rerun All] command to re-execute all operations before the operation (including this operation), or select [Stop] to stop the execution of the operation when the program is running. The stage specifies the process after the seed is run.

Out of date information can be displayed in the menu above the Flow , and you can view the specific reasons for the flow status out of date after clicking it . as follows:

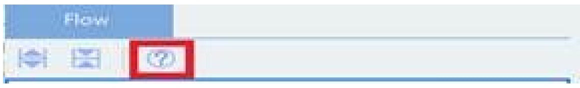


Figure 2-46 out of date button lights up

2.8 Set device

Part_settings are introduced as follows: Double-click [Sources] / [PGL50H] in [Navigator] or click Project Setting to pop up the device selection window, as shown in the figure below:

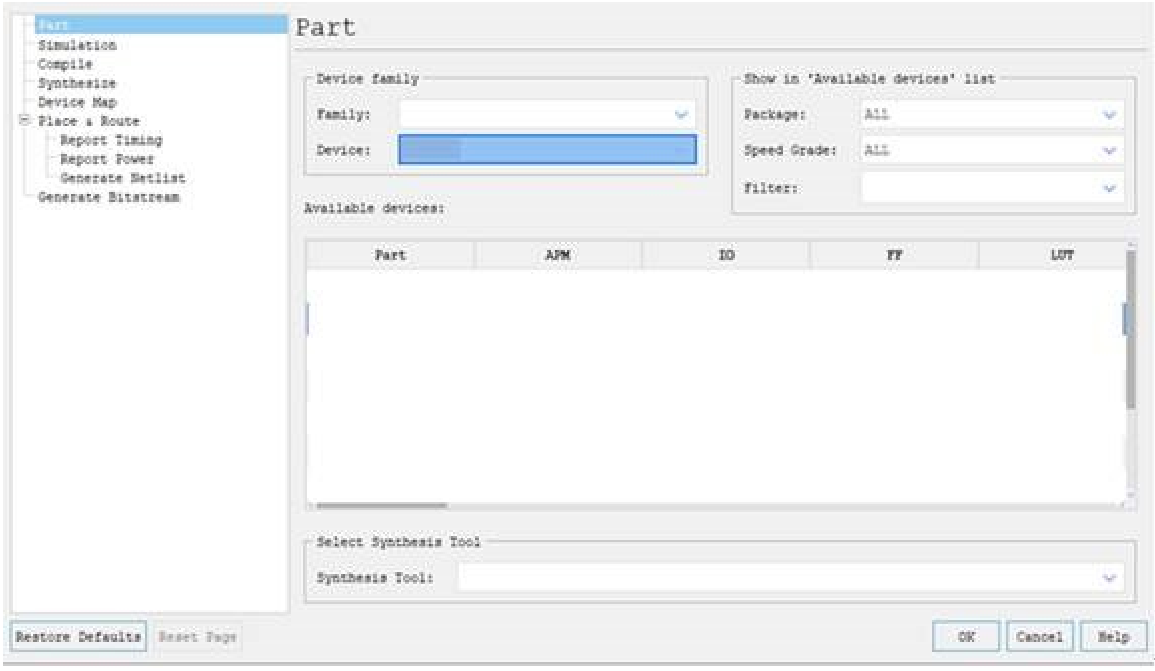


Figure 2-47 device selection window

【 Family 】 : select the device family;

【 Device 】 : select the device model;

【 Package 】 : Select the package type;

【 Speed Grade 】 : select the speed grade;

【 Filter 】 : filter devices according to the input;

【 Synthesis Tool 】 : Select the synthesis tool.

2.9 Add files

2.9.1 Add source file

Click the red button in the Figure below

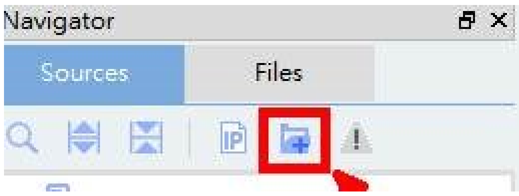


Figure 2-48 In the Sources window, click Add Source on the toolbar

Or right click on the red area in the figure below and click the Add Source menu

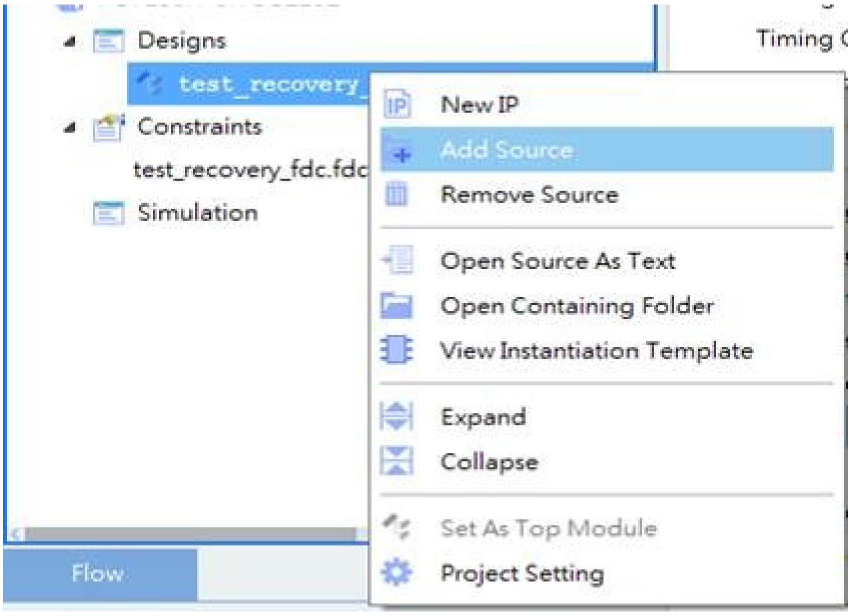


Figure 2-49 Add Source in the right-click menu in the Sources window

The following interface appears:

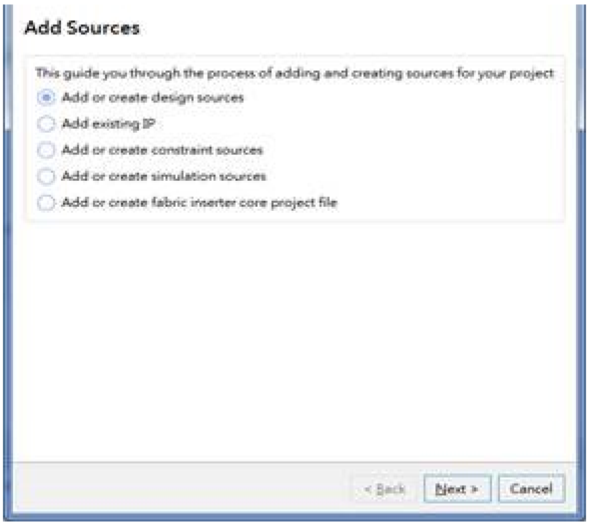


Figure 2-50 Add Source interface

Click Next , the following interface appears:

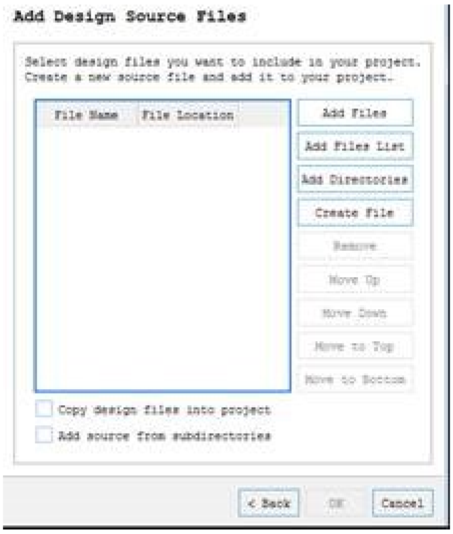


Figure 2 -51 Add design interface

When adding files, you can find the corresponding files to add through Add Files , or you can add files that meet the rules in the entire folder through Add Directories . If you check the " Add source from subdirectories " below, you will search for the selected directory Add all files that meet the rules in all subdirectories of . If the " Copy design files into project " option is checked, the program will copy the design file (add.v) to the source folder in the project directory. When copying, at least keep the first-level directory where the source file is located. After the design file is added, you will see the software interface as shown in the figure below:

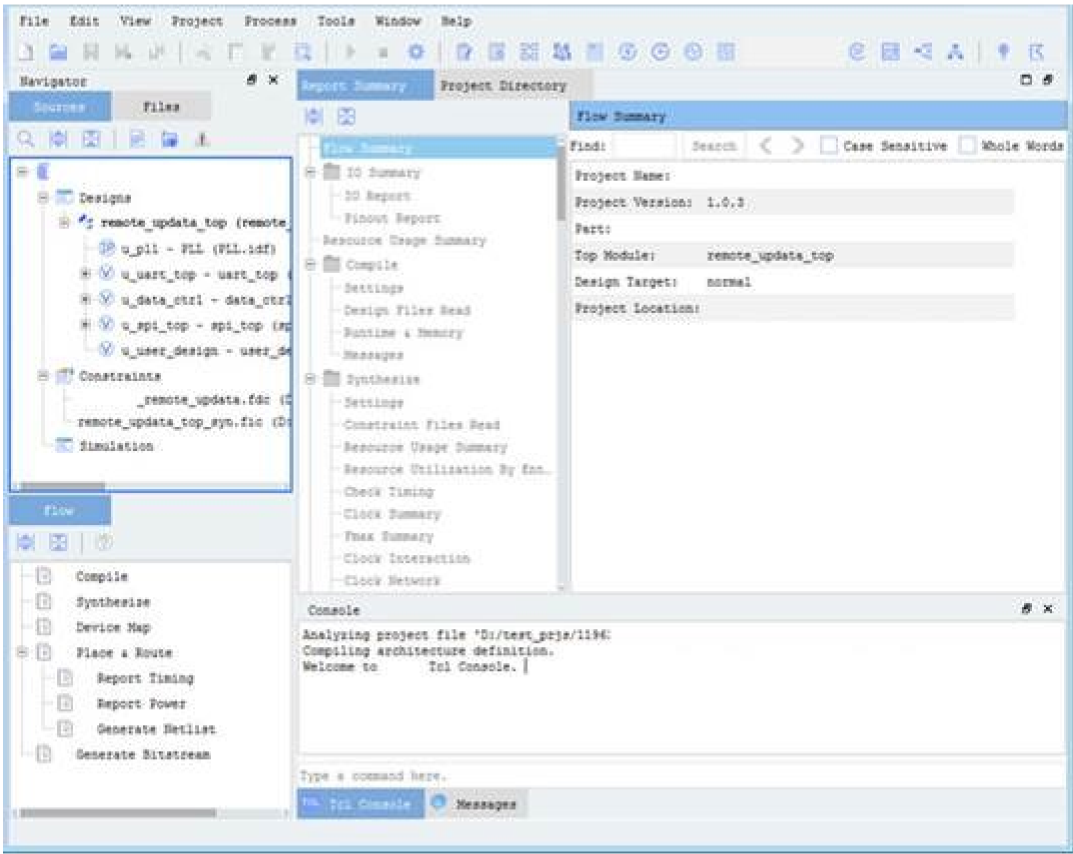


Figure 2-52 The software interface after adding design files

If adding files fails, the following prompt box will appear:

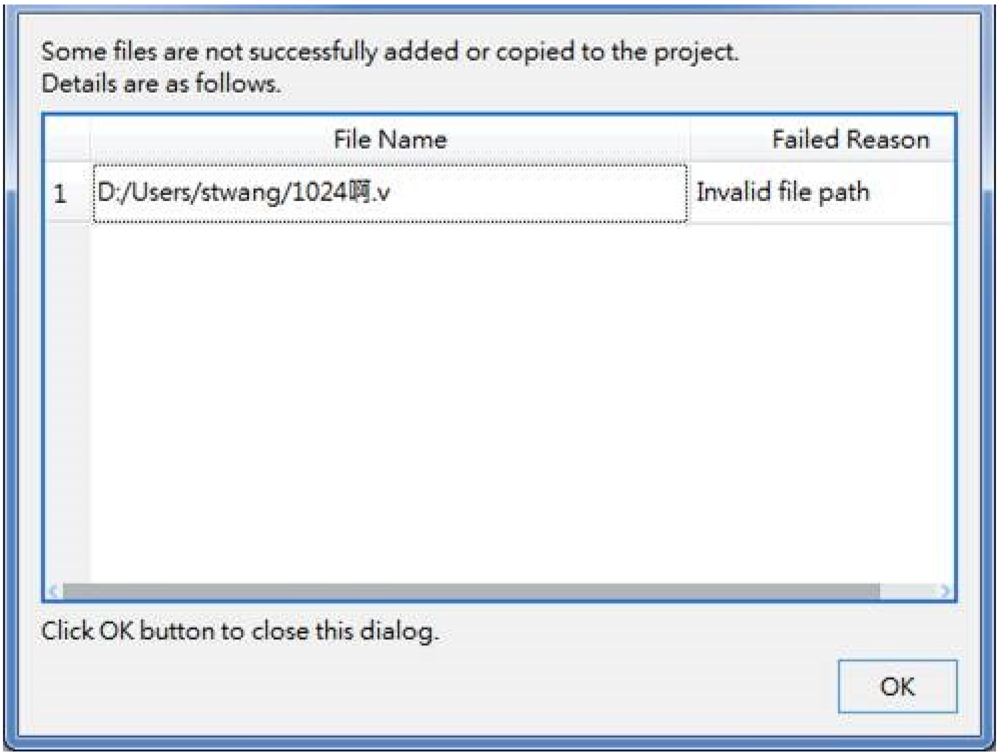


Figure 2-53 Add file failed dialog box

Reason for failure:

Invalid file path : The file path is too long or contains illegal characters (such as Chinese characters)

Copy file failed : Copy file failed

New file failed : failed to create a new file

[Files] in the project management area [Entry] displays the input files of the project, you can view the corresponding file path and type, and the right-click menu has operations such as edit file , open containing folder , show base name , etc., among which show base name can be Directly display the file name for easy viewing.

1) Search in user-added files

When searching for a keyword in the files added by the user, you can use the " Find In Files " tool in the toolbar to search, as shown in the figure below:



Figure 2-54 " Find In Files " toolbar position

After opening the tool, the interface is as shown in the figure below:

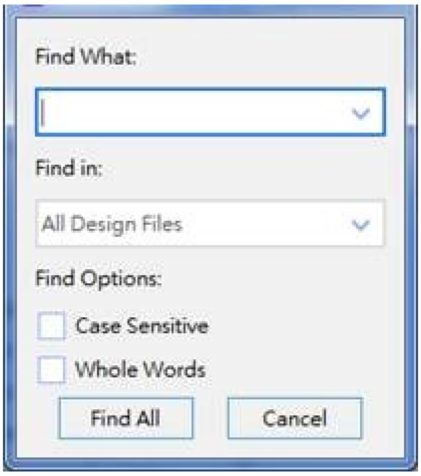


Figure 2-55 " Find In Files " tool interface

Among them, the drop-down box under the title of " Find in: " can specify the scope of the search. There are three selection ranges. The two check boxes under the title of " Find Options: " can specify the search method, including case sensitivity, and whether the whole word match, as shown in the figure below:

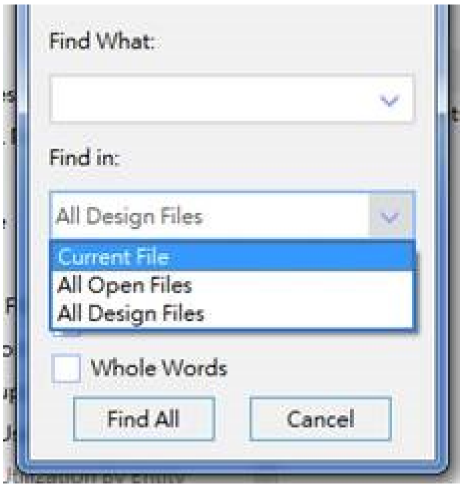


Figure 2-56 " Find In Files " tool search range

It can be seen that the tool has a total of three search scopes: " Current File " / " All Open Files " / " All Design Files ": " Current File " and " All Open Files " refer to the currently opened and Search in all open files, " All Design Files " refers to search in all user-added source files, regardless of whether these files are opened in a text editor;

The search results will be displayed in the Console window below the main interface, as shown in the figure below:

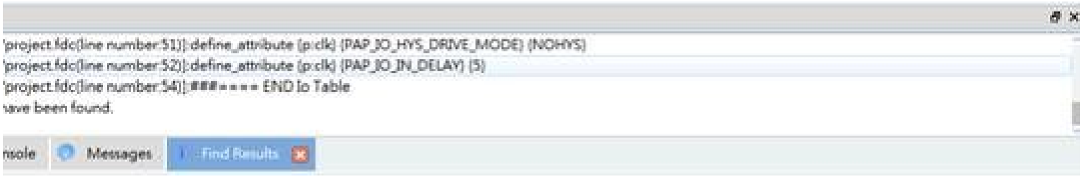


Figure 2-57 " Find In Files " tool search results

The search results include the name and line number of the searched files containing keywords, as well as the number of results.

2) IP file

[Add Sources] in the project management area to pop up the right-click menu, click Add Source , select the Add IP button in the dialog box that appears, and select *.idf in the drop-down list to add the corresponding ip file. (as shown in the following two Figures)

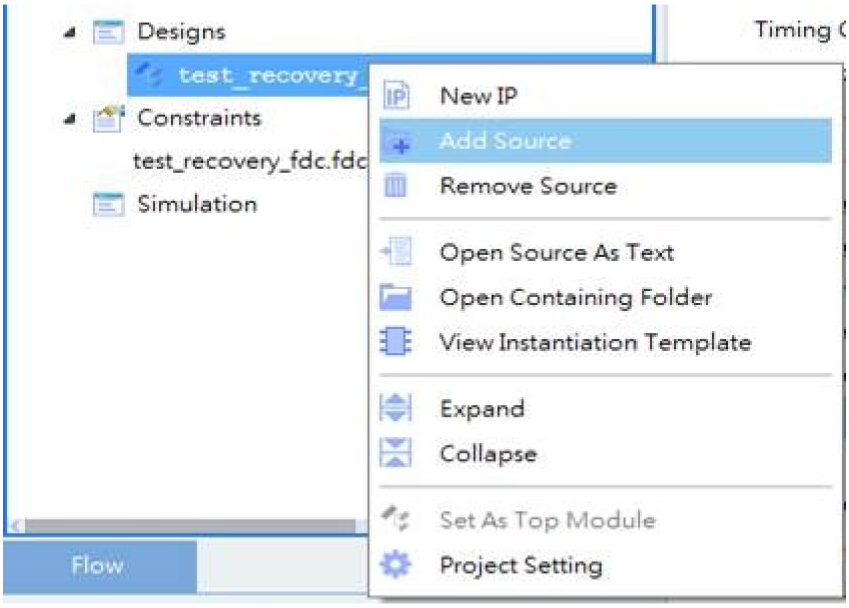


Figure 2-58 Add source file right-click menu

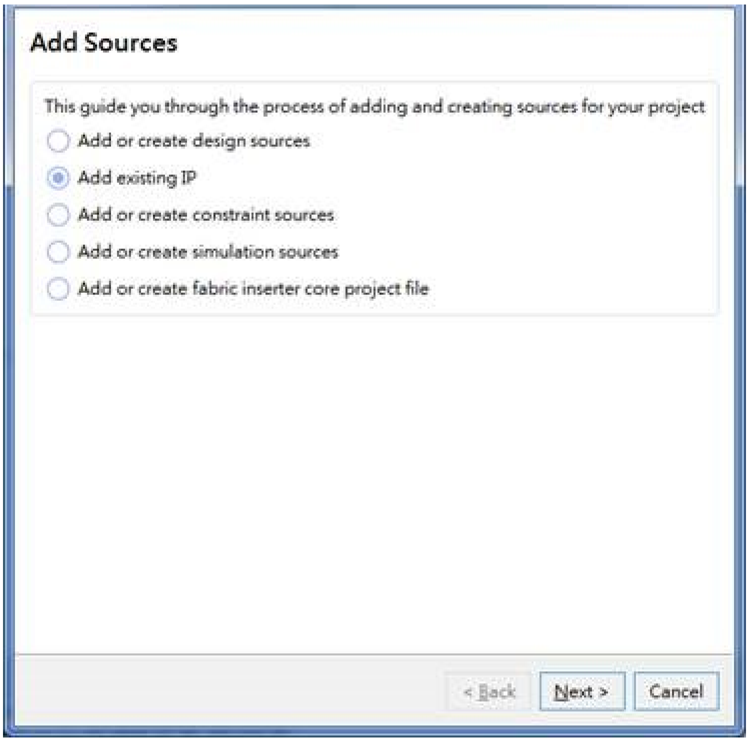


Figure 2-59 Add ip file dialog box

adding IP , the main interface is as shown in the figure below:



Figure 2-60 Main interface after adding IP

adding the IP , the rtl file hierarchy of the IP will be displayed on the sources interface (error ! Reference source not found.), but the rtl file is only displayed on the interface and not added to the project.

All rtl files contained in the IP will be automatically passed to the synthesis tool for synthesis, and users no longer need to add these rtl files of the IP to the design .

hierarchy supports identifying the IP instance that needs to be updated, which is reflected in the icon distinction in front of the module hierarchy . You can right-click to select the ip project file (multiple choices are allowed) , and click Regenerate IP to directly update the content of the IP file, as follows:

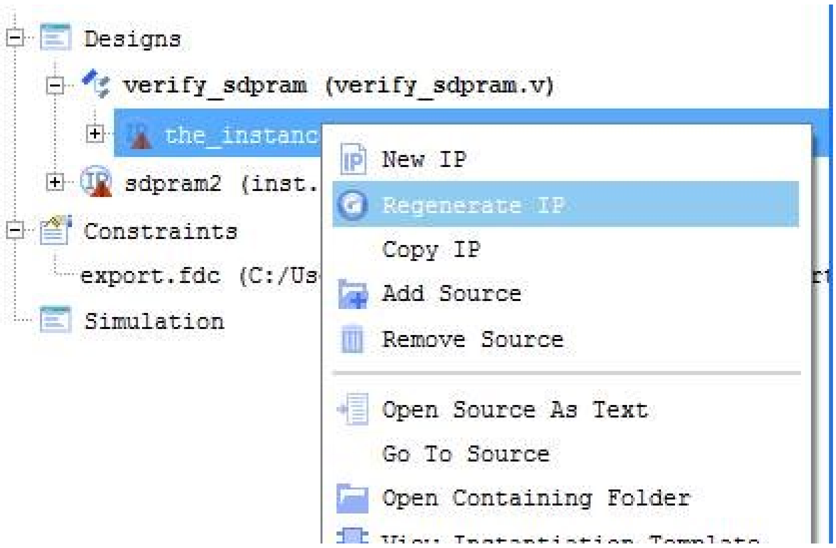


Figure 2-61 update IP interface

Right-click to select the ip project file and click Copy IP to copy the ip project file and add it to the project. After setting the IP name and target path, you can execute the copy operation. After the copy is completed, you can configure it, as follows:

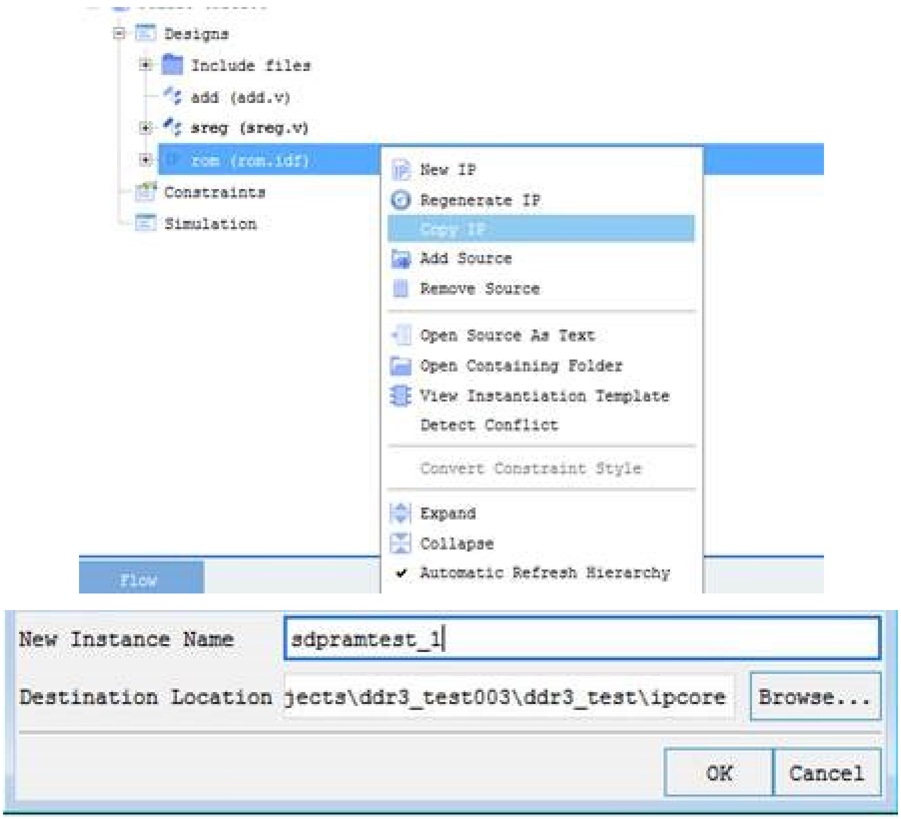


Figure 2-62 Copy IP interface

2.9.2 New source file

The previous operation is similar to adding source files, when the following interface appears:

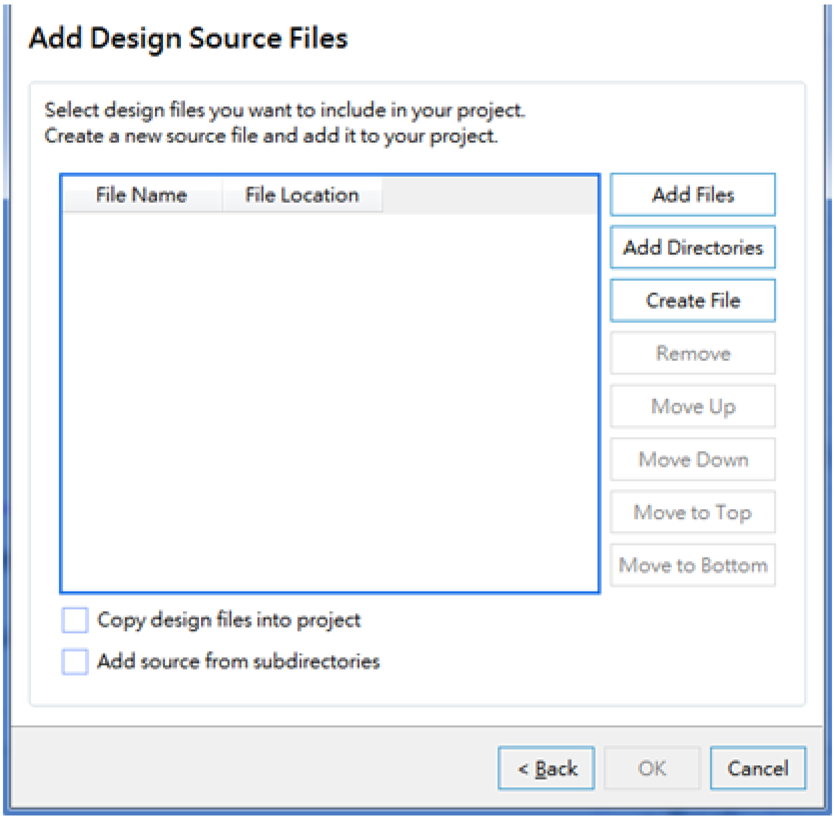


Figure 2-63 Add source file main interface

Click the Create File button, and the following interface will appear:

Click the drop-down list above to select the type of new file:

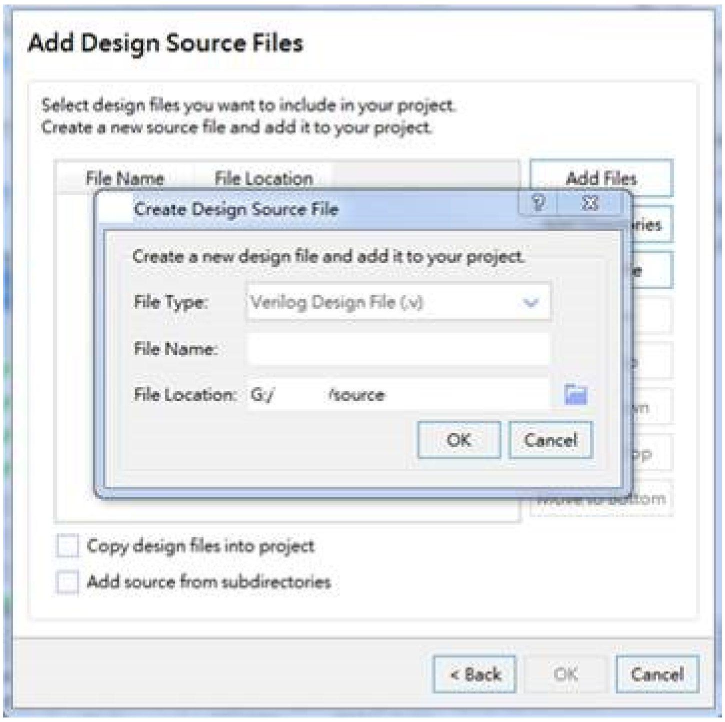


Figure 2-64 After clicking Create File , an interface pops up

After selecting the file type (select .V file here), enter the file name in the text box below and select the file path:

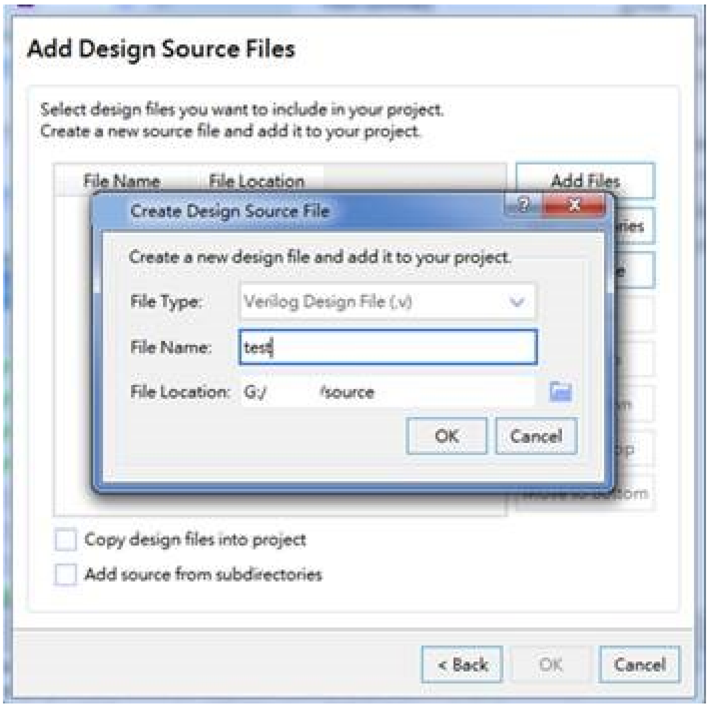


Figure 2-65 input file name interface

If the file name already exists, a pop-up window will prompt and ask whether to rename as follows:

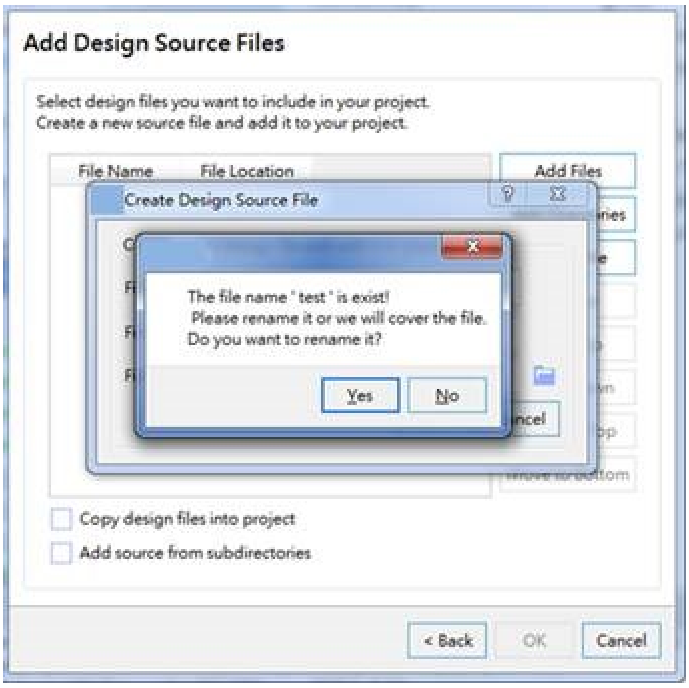


Figure 2-66 Input file name duplicate name prompt interface

If you select ' Yes ', return to the above interface to rename, if you select ' No ', the new file will overwrite the previous file with the same name.

clicking OK , the following interface appears:

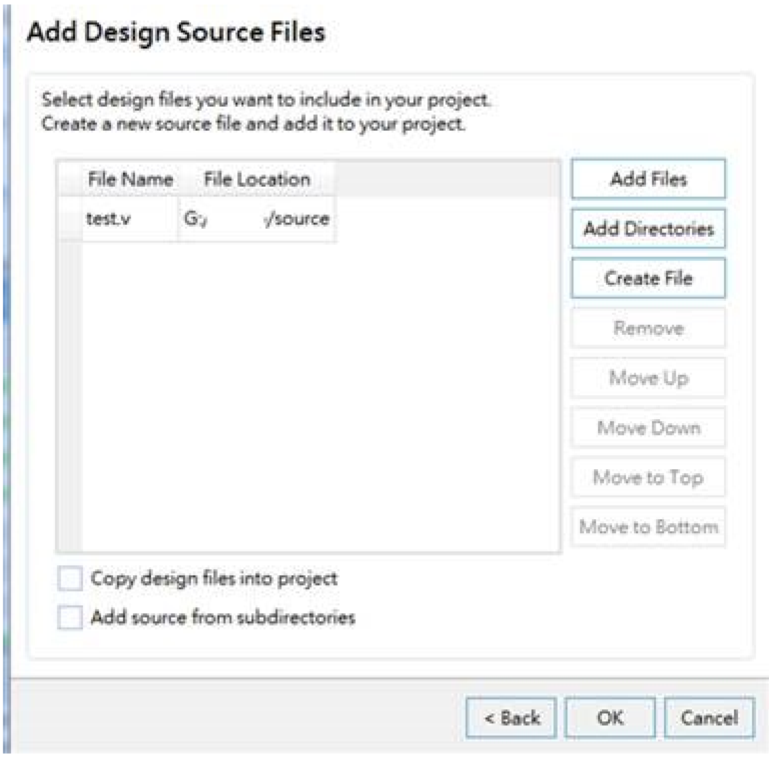


Figure 2-67 Interface after Create File ends

Multiple files can be added or created here. Click OK after adding or creating a new one :

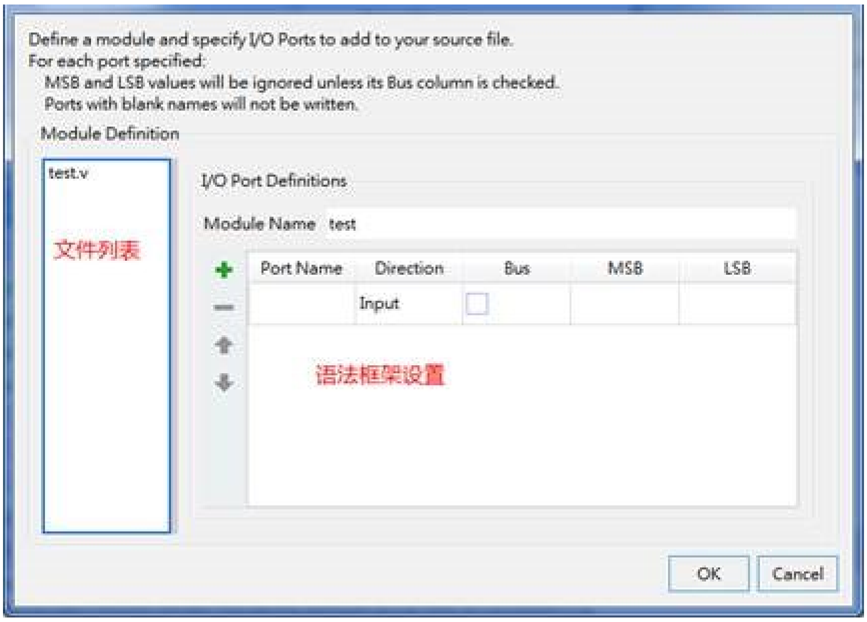


Figure 2-68 .v file syntax frame setting interface

In the file list, you can select the file you want to set, and in the syntax frame setting area, you can set it according to your needs:

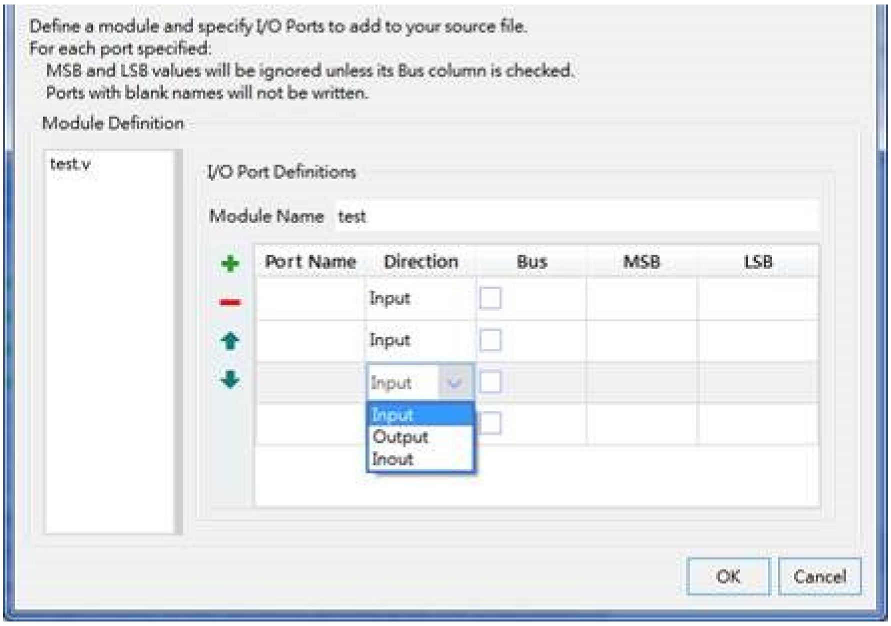


Figure 2-69 module setting interface

After the setting is complete, click OK , and the newly created file will be opened:

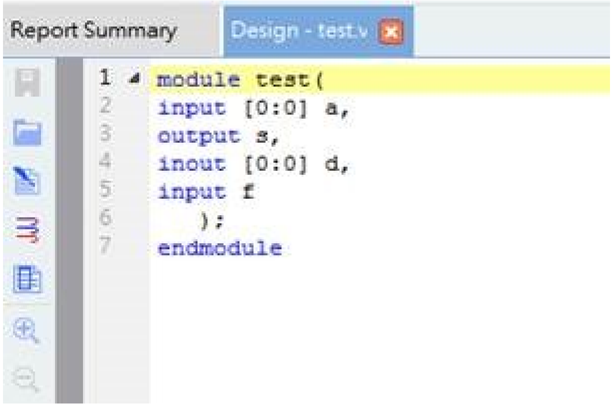


Figure 2-70 .v file to generate the interface after setting the grammar framework

.VHDL file is basically the same as the .V file, except for the difference in the setting interface:

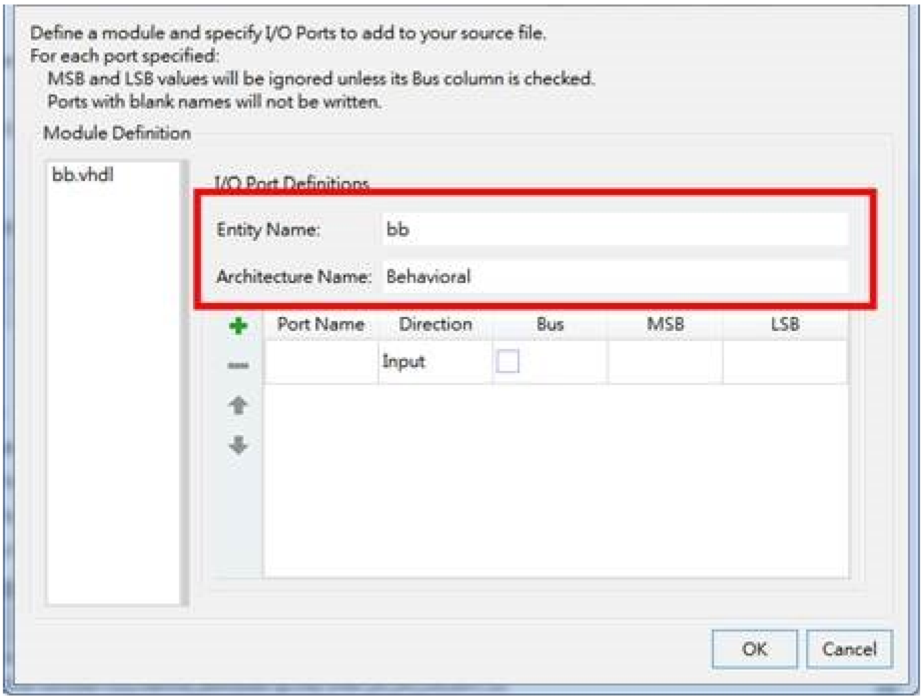


Figure 2-71 Syntax frame setting interface of .vhdl file

Due to the difference in syntax, the content in the red box is different from the .V file. The same is true for the final generated file:

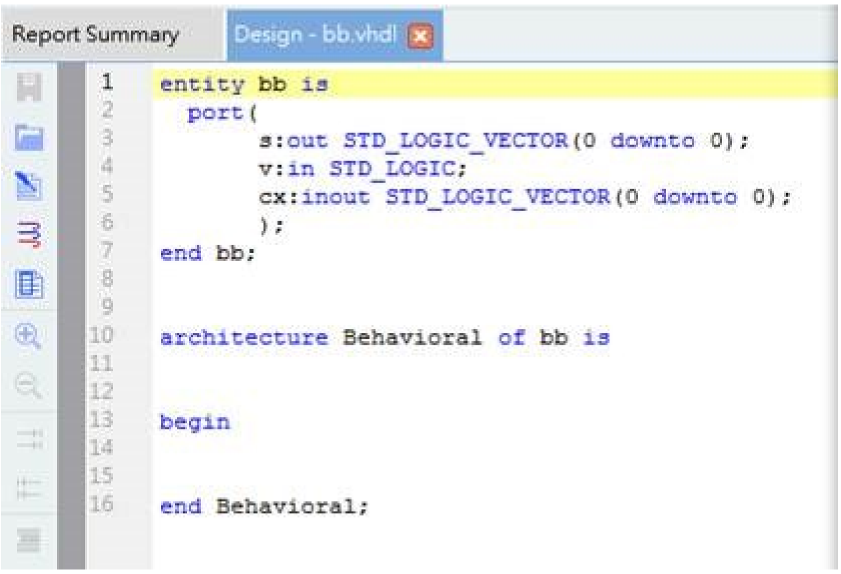


Figure 2-72 The interface after the .vhdl file is set

2.9.3 Refresh the design hierarchy

Right click on the source window, the following interface will pop up

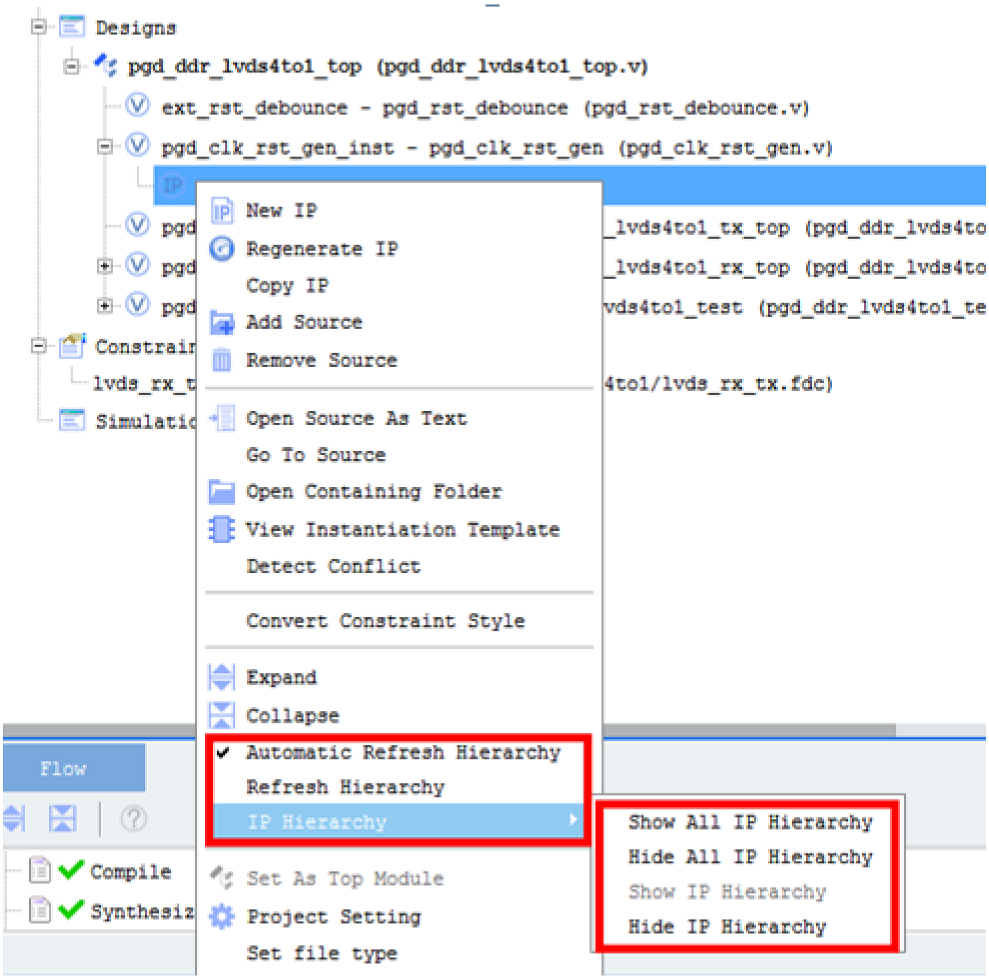


Figure 2-73 refresh hierarchy

[Automatic Refresh Hierarchy]: Automatically refresh the hierarchy of the design when there are addition, deletion, or modification operations in the design file. The default is checked.

When unchecked, when the design file is newly saved, the " Hierarchy is out of date " prompt and the Reload button will pop up under Sources , and the design hierarchy will be refreshed when the Reload button is clicked .

【 Refresh Hierarchy 】: Manually refresh the design hierarchy .

【 IP Hierarchy 】 : Control whether to display the hierarchical structure of IP , including the following four functions:

(1) Show All IP Hierarchy: Set the hierarchical structure of all IPs to expand

(2) Hide All IP Hierarchy: Set the hierarchical structure of all IPs to be unexpandable

(3)Show IP Hierarchy: Expand the selected IP hierarchy

(4) Hide IP Hierarchy: Hide the selected IP hierarchy

2.9.4 Global include setting

Set global include and clear global include in the right-click menu bar of the source window of PDS to perform related operations on the selected files; the entry of set global include and clear global include is not visible in the OEM process and back-end version.

Set the target file as global include , all design files can use the macro defined in the target file, which will cause the relevant macros of the design file to take effect, resulting in different analysis results.

Clear the target file from the global include , all related macros of the design file without the include target file will be invalid, and different analysis results will be produced.

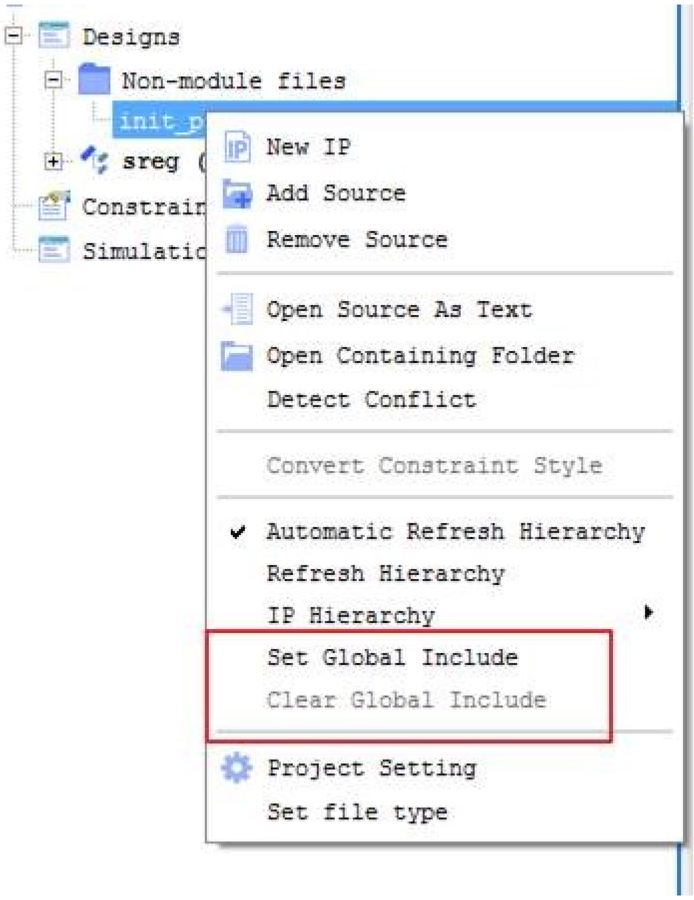


Figure 2-74 set Global include

2.9.5 Add constraints file

User design constraints include timing constraints and module location constraints. The corresponding constraint files are divided into two types, timing constraints and physical constraints. The following is an introduction to the constraint file formats supported by pds .

Sdc format file: This format is a timing constraint file format. This format file can only be loaded without using a synthesis tool. It records timing -related constraint information.

Lcf format file: This format is a logical constraint file format. This format file can only be loaded without using a synthesis tool. It records information related to logical constraints, such as setting attributes. After Mapping , part of the logical constraint information will be converted into physical constraints.

Scf format file: This format file records timing -related constraint information, which can be added with or without comprehensive tools, and is used in the dev_map stage.

Fdc format file: This format file contains timing and logic constraints, which can only be used when a synthesis tool is used.

1) Add user constraints file

Click the red button in the Figure below

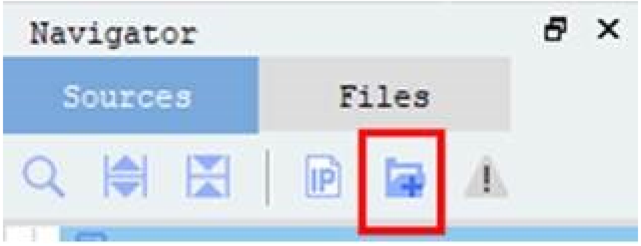


Figure 2-75 Add constraints file

Or right click on the red area in the figure below and click the Add Source menu

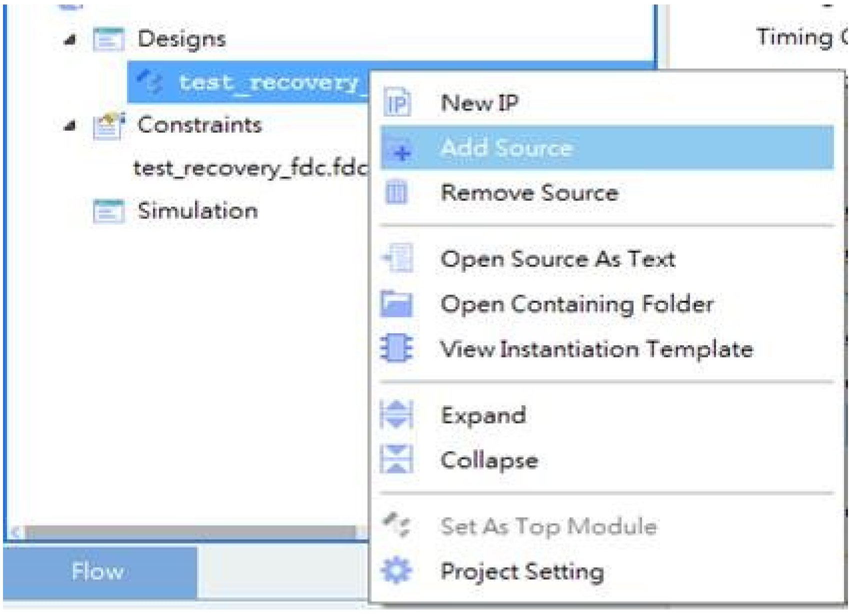


Figure 2-76 Right-click menu to add source files

The following interface appears:

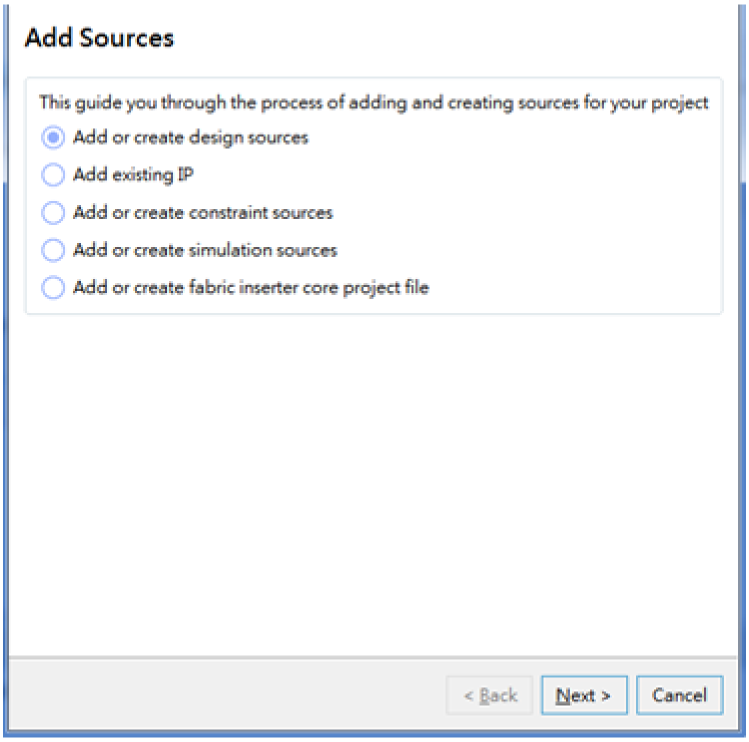


Figure 2-77 Add source file interface

Select the third item Add or create constraint sources , as shown below:

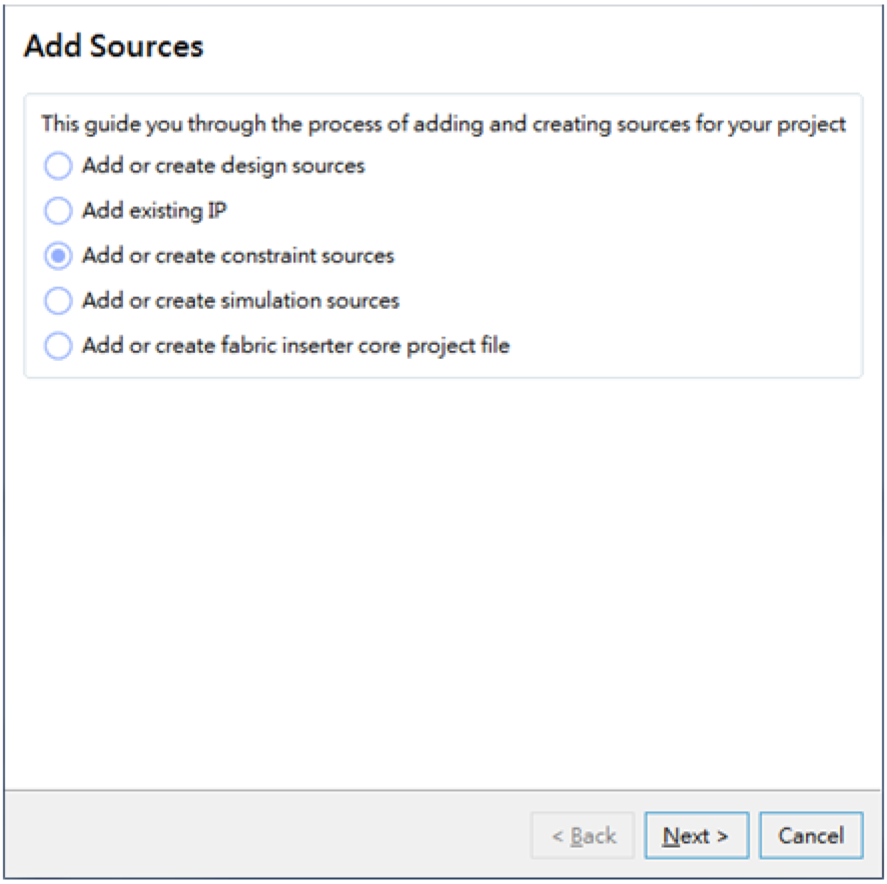


Figure 2-78 choose to add constraints interface

Click Next , the following interface appears:

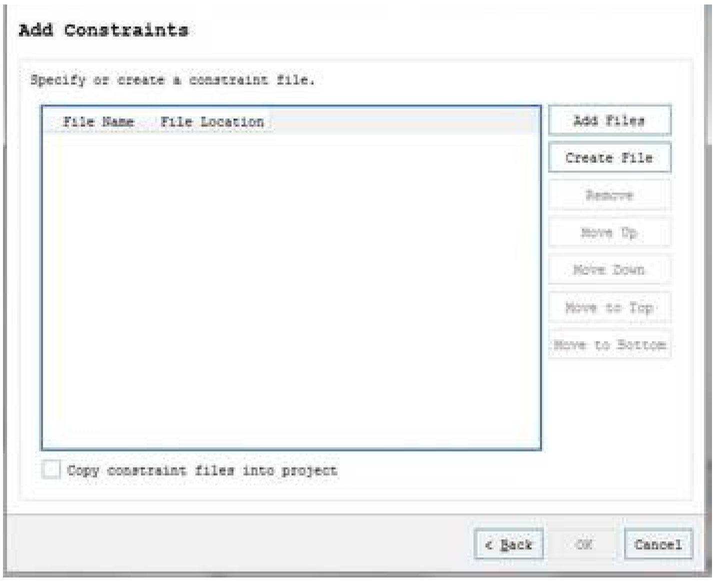


Figure 2-79 Add user constraint files

After selecting a constraint file or creating a new constraint file, click OK to join the project. Similarly, when the " Copy constraint files into project " option is checked, the program will copy the constraint files to the source folder in the project directory.

Constraint files (.sdc files) have the following format:

Command format: create_clock –name clock_name –period clock_period -waveform { 0 wave_period } [get_ports { clock_port_name }]

Where clock_name is the clock name corresponding to the clock port to be constrained (clock_port_name in design) (in timing analysis); clock_period is the period of the clock to be constrained; wave_period is the amplitude of the clock to be constrained (generally the duty cycle is 50%), whose value is half of the clock period (wave_period=clock_ period/2); clock_port_name is the clock port to be constrained (in design).

Note: clock_name and clock_port_name can be different, but when creating a clock constraint, it is recommended that clock_name be the same as clock_port_name so that clock_name and clock_port_name are the same for easy correspondence and viewing.

Suggestion: (especially for multi-clock constraints) add "#Begin clock constraint" before each clock constraint and "#End clock constraint " at the end to show the difference between different clock constraints.

Example: Now to constrain the clock port clk in the design , you can create a clock named clk with a period of 6.929ns and a duty cycle of 50% , then the sdc file can be edited as:

#Begin clock constraint (this statement can be omitted)

create_clock -name clk -period 6.929 -waveform { 0 3.4645 } [get_ports { clk }]

#End clock constraint (this statement can be omitted)

In particular, when there is "[ ]" in the clock name (bit operation for multi-bit clocks), "{}" should be used to enclose the entire clock name;

Example: Now to constrain the clock port clk[0] in the design , you can create a clock named clk with a period of 6.929ns and a duty cycle of 50% , then the sdc file can be edited as:

#Begin clock constraint (this statement can be omitted)

create_clock -name {clk[0]} -period 6.929 -waveform { 0 3.4645 } [get_ports { clk[0] }]

#End clock constraint (this statement can be omitted)

2) Add Physical Constraints File

Physical constraints files are added through the Physical Constraint Editor window. Opening the Physical Constraint Editor window requires running Device Map . So the actual operation to add the physical constraint file can be placed after the Device Map is running.

Physical Constraint Editor window can be accessed through the Physical Constraint under the Tools menu

Editor (Post-Map) opens, or directly through the Physical Constraint Editor (Post-Map) shortcut in the toolbar . The secondary menu under Tools in the menu bar is shown in the figure below:

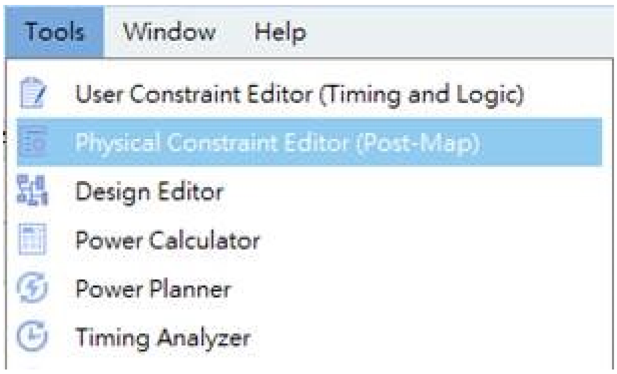


Figure 2-80 Physical Constraint Editor (Post-Map) under the Tools menu

Click the above menu in PDS , and the Input Physical Constraint File window will pop up. In this window, Current pcf file indicates the pcf file in the current project , and options such as Delete pcf

from project and Select a pcf to edit provide operations for deleting, editing, adding and replacing pcf files.

The window for adding a physical constraint file is shown in the figure below:

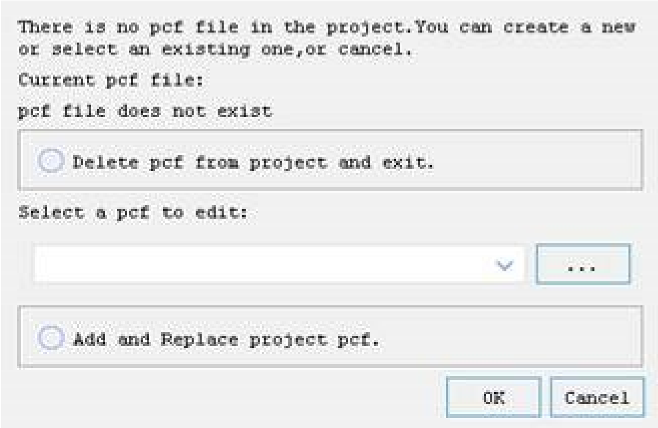


Figure 2 -81 Add physical constraints

Click the OK button and the Physical Constraint Editor (PCE) will start . The opened Physical Constraint Editor interface is shown in the following figure:

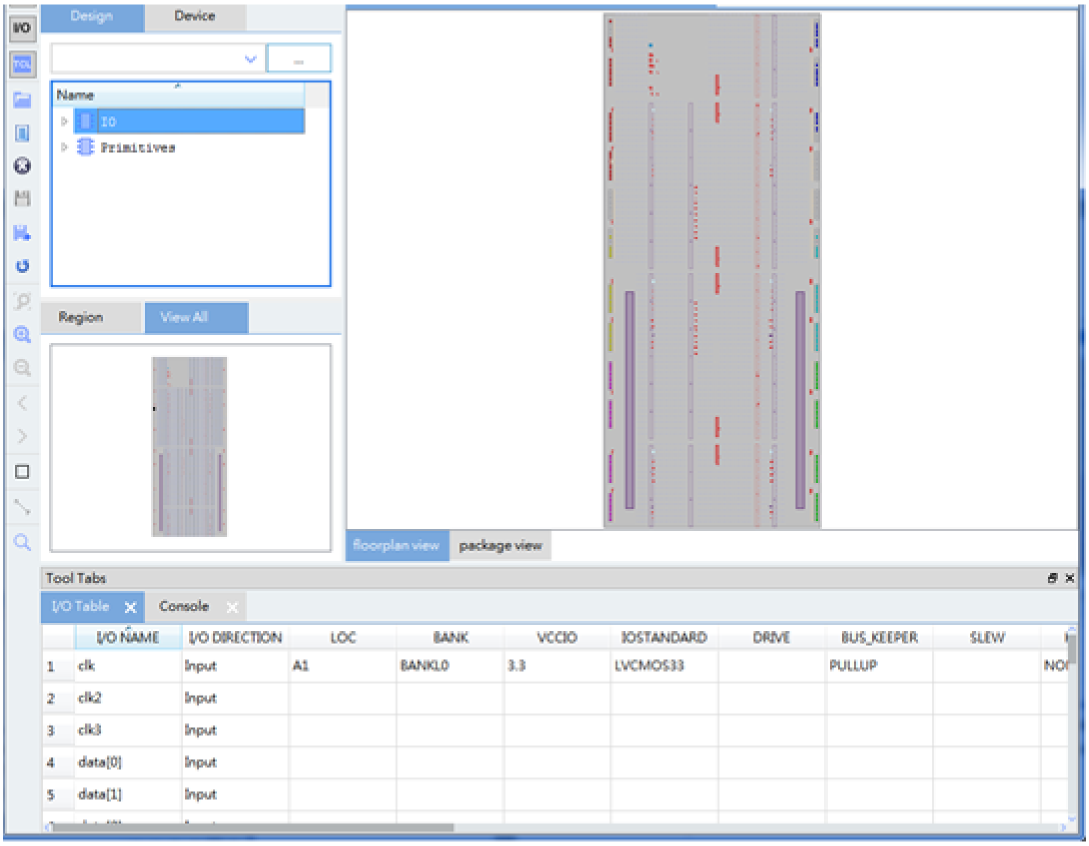


Figure 2-82 Physical Constraint Editor interface after adding physical constraints

After the physical constraint file is added, close the Physical Constraint Editor interface to return to the main interface.

Physical constraints can be divided into pin constraints and layout constraints. The software provides pin constraints and layout constraints commands, both of which support writing physical constraint files and generating corresponding physical constraint files through graphic operations in Constraint Editor .

i. Pin constraints

a. Edit the pin assignment file

The pin constraint file can well support the standard form (without setting pin attributes) constraints, and the function of setting pin attributes (optional) is also gradually improved. There are two formats of pin constraints, including the def_port command and the def_inst_site command, and the two are only different in the format header (def_port and def_inst_site), and the rest of the formats are the same.

def_port command

def_port port_name LOC=pin_loc

[IOSTANDARD=io_standard_name]

[SLEW=SLOW/FAST]

[DRIVE=2/4/6/8/12/16/24]

[PULLDOWN=TRUE/FALSE]

[PULLUP=TRUE/FALSE]

[KEEPER=TRUE/FALSE]

[IODELAY=NONE/BOTH/IBUF/IFD]

Among them, port_name is the name of the IO port to be constrained (in design) ; pin_loc is a pin resource location on the chip ; io_standard_name is the name of various port standards; the possible values of SLEW are SLOW and FAST; the desirable values of DRIVE The values are 2 , 4 , 6 , 8 , 12 , 16 and 24; the possible values of PULLDOWN , PULLUP and KEEPER are TRUE and FALSE; the possible values of IODELAY are NONE , BOTH , IBUF and IFD . In this command, everything in square brackets is optional. Among them, for input ports, the SLEW and DRIVE options are unavailable; for output and bidirectional ports, the IODELAY option is unavailable.

Example 1 :

a counter user design, there is a clock input port named clkin , which is bound to the pin of A11 . then use the standard form (without optionals) constraints as follows:

def_port clkin LOC=A11

Note: For input ports, the SLEW and DRIVE options are not available; for output and bidirectional ports, the IODELAY option is not available.

Example 2 :

a user design named counter , there is a clock input port named clkin , which is bound to the pin of A11 , and its pin properties are set. The content is as follows:

def_port clkin LOC=A11 IOSTANDARD=LVTTL IODELAY=NONE

If the name of an output port is LED1 , bind it to the pin of B17 and set its pin properties. The content is as follows:

def_port LED1 LOC=B17 IOSTANDARD=LVCMOS18 SLEW=FAST DRIVE=16

def_inst_site command

def_inst_site port_name pin_loc

Among them, port_name is the name of the IO port to be constrained (in design) ; pin_loc is a pin resource location on the chip , and supports three description methods: IOB , PIN , and PAD ;

Example 1 :

a counter user design, there is a clock input port named clkin , which is bound to the pin of IOB_9_42 by IOB description . The content is as follows:

def_inst_site clkin IOB_9_42

Example 2 :

a counter user design, there is a clock input port named clkin , which is bound to the pin of P1 by PIN description . The content is as follows:

def_inst_site clkin P1

Example 3 :

a counter user design, there is a clock input port named clkin , which is bound to the pin of PAD1 in the way of PAD description. The content is as follows:

def_inst_site clkin PAD1

b. Graphics operations generate pin constraint files

The software provides the function module package of the underlying IO constraints . After the software runs the map , the underlying mapping netlist has been obtained, and these underlying IOs can be directly operated to realize the underlying IO operations.

The software provides a graphical pin constraint function, Pin assignments can be performed on three types of views: package view or floorplan view , I/O Table and Design Browser . The I/O Table view can be operated independently, but the package view or floorplan view and Design Browser view must be used together. The final result of the two methods is the same, but the operation form of the constraint is different. In addition , the instance of the IO type in the package view or floorplan view , the io in the Design Browser>>IO view, and the io in the I/O Table view are all in one-to-one correspondence.

Users can perform pin constraints by dragging and dropping in the view. Drag and drop the io in the Design Browser>>IO view to the pin in the package View or the IOB in the floorplan view , or fill in the constraint position (LOC) of the IO (I/O Name) in the I/O Table view , To complete the pin constraints. As shown below:

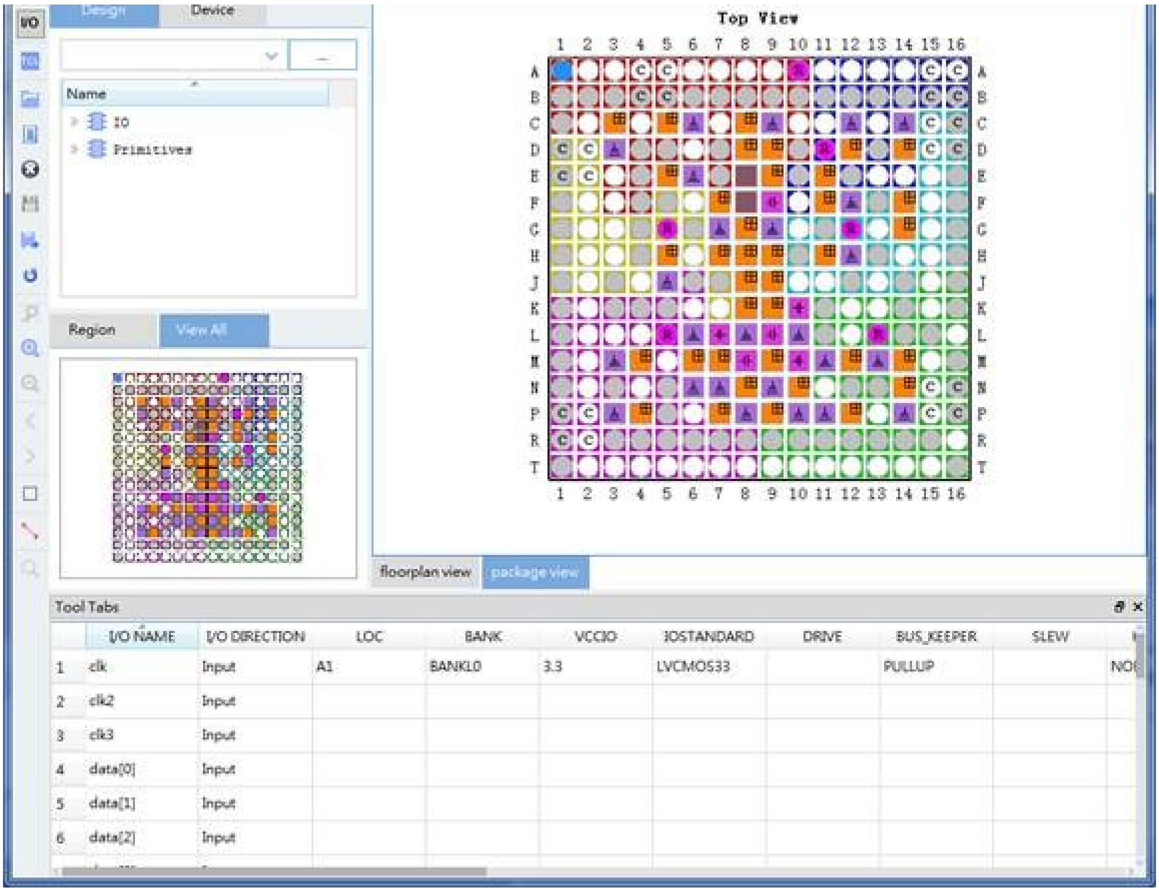


Figure 2-83 Pin constraint view

Note: No matter which method is used to complete the pin constraints, all views will reflect the pin constraints according to the corresponding rules.

ii. layout constraints

a. Edit layout constraints file

The def_inst_site command is generally used to edit the layout constraint file , and the format is as follows:

command format : def_inst_site inst_name site_name[impl_name]

Among them, inst_name is the name of the design instance to be constrained. If the design instance is IO type, it is consistent with the pin constraint (this is also the relationship between pin constraint and layout constraint); site_name is the name of the device resource in the FPGA chip , such as CLMA_74_14, MUL_71_22 , etc.; impl_name is optional, indicating the basic physical unit that the corresponding design example must use (such as FGA, FGB, FF1 , etc. in CLMA).

Example 1 :

Suppose TempInst is an instance of type LUT4 in the design netlist, and you want to put it on CLMA_77_38 . Then the command is:

```
def_inst_site TempInst CLMA_77_38
```

Since LUT4 has two implementations of FGA and FGB on a CLMA , if you want to specify F to implement TempInst . Then the command is:

```
def_inst_site TempInst CLMA_77_38 F
```

Example 2 :

Assuming that TempFF is an instance of a register type in the design netlist, you want to put it on CLMA_77_35 and use FGA to implement it. The command is:

```
def_inst_site TempFF CLMA_77_35 FGA
```

Example 3 :

Suppose TmpMem is an instance of a BRAM type in the design netlist , and you want to put it on BRAM_71_39 . Then the command is:

```
def_inst_site TmpMem BRAM_71_39
```

Example 4 :

Suppose TmpMul is an instance of the MUL type in the design netlist , and you want to put it on MUL_71_38 . Then the command is:

def_inst_site TmpMul MUL_71_38

b. Graphics operations generate layout constraint files

The software provides the function module floorplanner of the bottom unit layout . After the software runs the map , the bottom mapping netlist is generated, and these bottom units can be directly operated to realize the layout operation of the bottom layer.

Layout constraints are completed by two views, floorplan View and Design Browser . Users can drag and drop instances in Design Browser>>Instance view to floorplan View to constrain the instance to the appropriate chip (resource) position. As shown below:

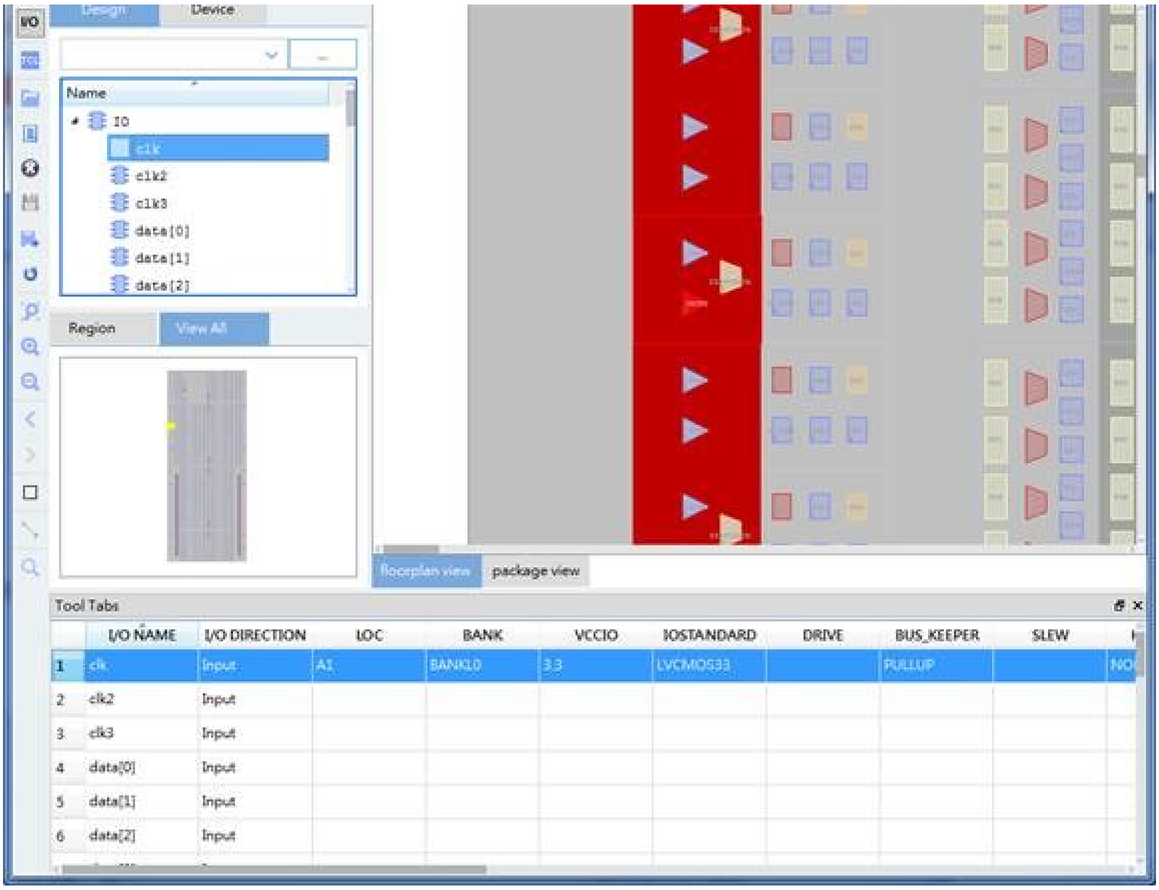


Figure 2-84 layout constraints view

iii. Regional constraints

The area constraint is actually a deformation of the layout constraint, that is, the layout constraint is not directly placed on a specific physical unit, but an area is specified in advance, and then the

software automatically places the layout constraint on any physical unit in the specified area according to the actual situation.

Two command forms for region constraints , including def_region command and def_inst_region command. The def_region command is used to define the layout area in the current FPGA chip; the def_inst_region command is used to constrain the design instance in the current design to a certain area.

a. Define the area

def_region command

Area constraints need to follow the principle of first declaring and then using, that is: first define the area and then use the area. For example, first create a region through the def_region command, and then put the instance into the region through the def_inst_region command .

def_region region_name xmin xmax ymin ymax

Where region_name is the name of the region for future reference ; xmin, ymin are the XY coordinates of the lower left corner of the region , xmax, ymax are the XY coordinates of the upper right corner of the region. In the FPGA chip, each physical unit has a coordinate, which can be seen in the floorplan View view. As shown below:

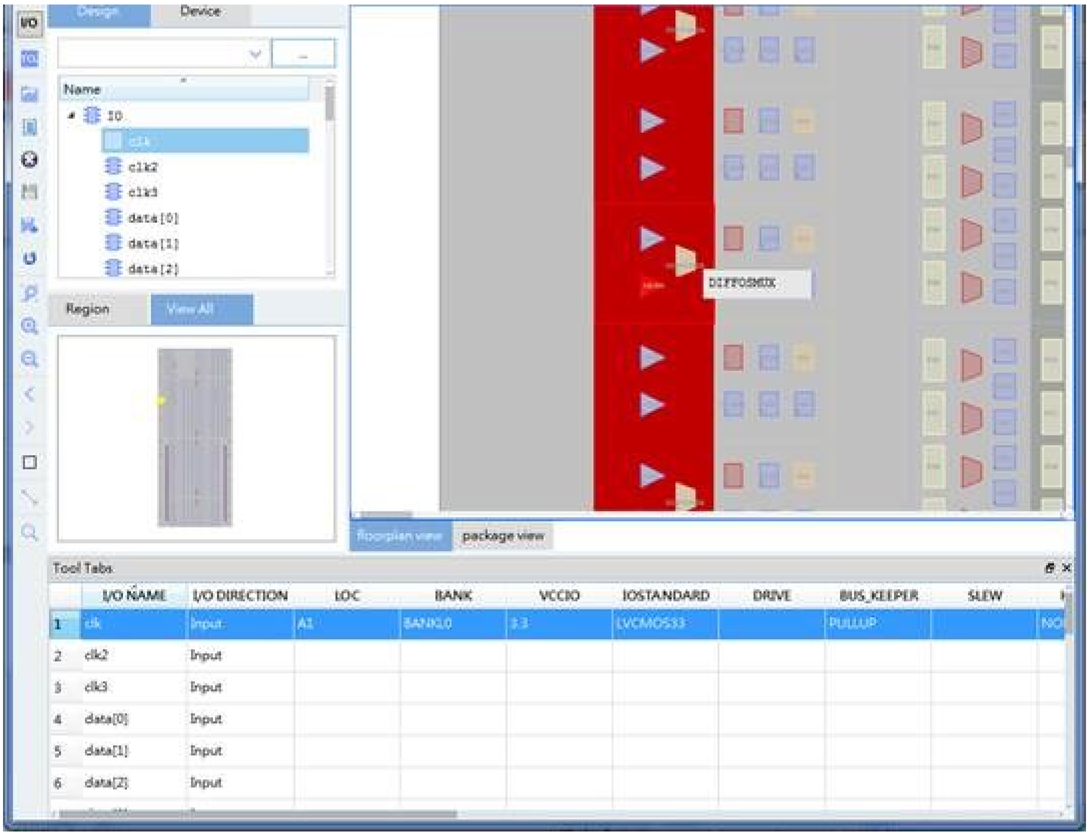


Figure 2-85 layout constraint view

When the mouse is placed on a blank space in a CLMA unit, the mouse tip gives the name of the CLMA unit CLMA_5_133 and its coordinates (4,44), which are the coordinates used in the def_region command.

Example:

Define a rectangular area reg1, the graphic display of this area is CLMA_190_11 in the lower left corner , the coordinates are (62,5); the upper right corner of the rectangle is CLMA_201_12, and the coordinates are (65,6).

with the def_region command is:

def_region reg1 62 65 5 6

b. Constraint Design Example

def_inst_region

When using this command, the user needs to define the command before it can be used. The command format is as follows:

def_inst_region inst_name region_name

where inst_name is the name of the design instance to be constrained in the netlist file, and region_name is the name of a region (defined by the above two commands). This command puts the instance inst_name into the region region_name during layout .

Example: Suppose TmpInst is an instance of type LUT4 in the design netlist , and you want to put it in reg1 defined by the previous two commands . The command is:

def_inst_region TmpInst reg1

2.10 Remove file

For the added file, you can select the file, click the right button, and use the pop-up right button 【 Remove Source 】 menu to remove the file. As shown below

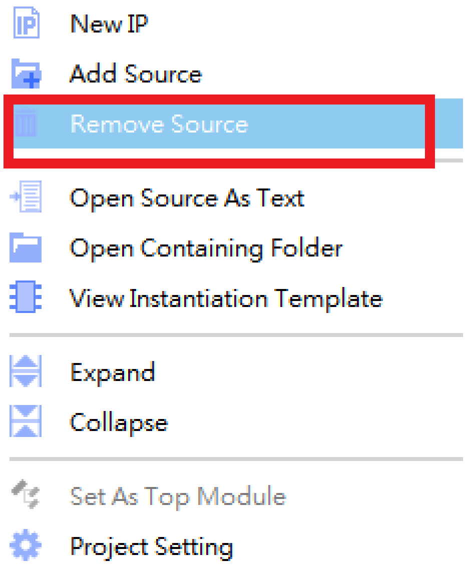


Figure 2-86 file removal menu

Click [Remove Source], and a dialog box as shown in the figure below will pop up. If you check " Also delete the project local file/directory from disk ", the deleted file will be deleted from the project, and the files in the disk will also be deleted.

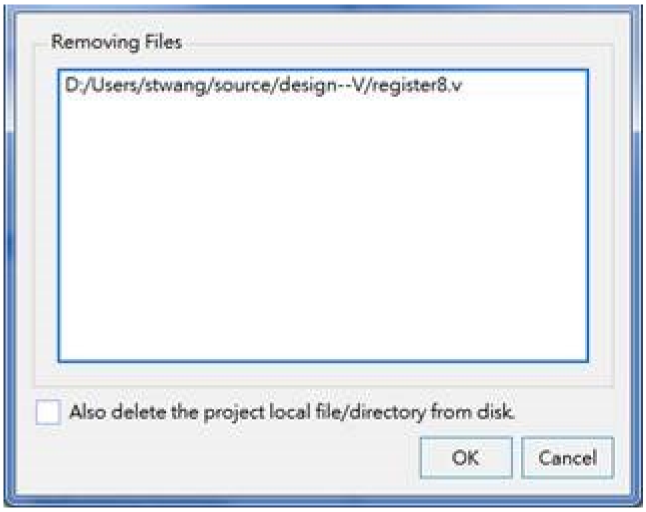


Figure 2-87 file removal dialog box

Select the design source file in Figure 2-85 , and there are other functional options in the right-click drop-down menu besides the operation of removing the file. The function is introduced as follows:

New IP : Add IP file; right-click the drop-down menu to select New IP , and the New IP dialog box will pop up to complete the addition of IP .

Add Source : Add a source file or a constraint file; right-click the drop-down menu and select Add Source or Project->Add Source to open the Add Sources dialog box to add files;

Open Source As Text : Open the file with the built-in text editor of PDS ;

Remove Source : delete the source or constraint file; select the source or constraint file, right-click the drop-down menu and select Remove Source to delete the file.

Open Containing Folder : Open the directory where the file is located.

Expand All : Expand all files.

Collapse All : Files are displayed collapsed.

Set As Top Module : Set the top module ; select the module of the source file in the Designs structure , right-click the drop-down menu and select Set As Top Module , you can set the selected module as the top module .

Physical constraint files are removed by opening the Delete from project option in the Physical Constraint Editor window . As shown below:

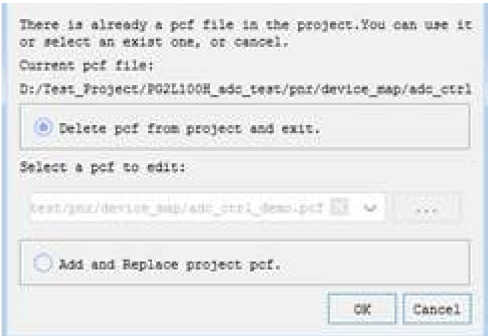


Figure 2-88 pcf files removed

2.11 Parameter settings

The option configuration window [Project Setting] of the software flow , and then you can make specific settings. Generally, there are two ways to open 【 Project Setting 】 .

a . Click on the Project menu Project Setting , you can set parameters. As shown below:

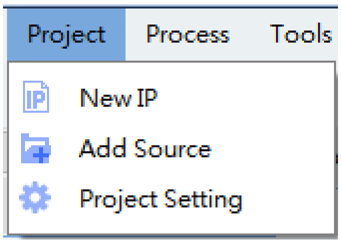


Figure 2-89 Configure menu

b . In the right-click menu of the project management area, select Project Setting to set parameters. As shown below:

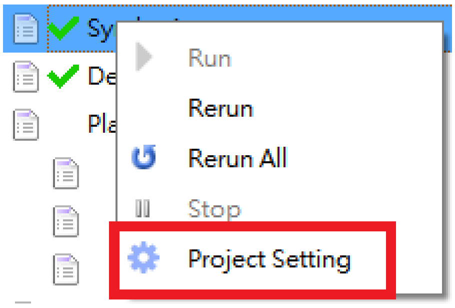


Figure 2-90 project management area configure menu

The option configuration window [Project Setting] of the software flow , as shown in the figure below :

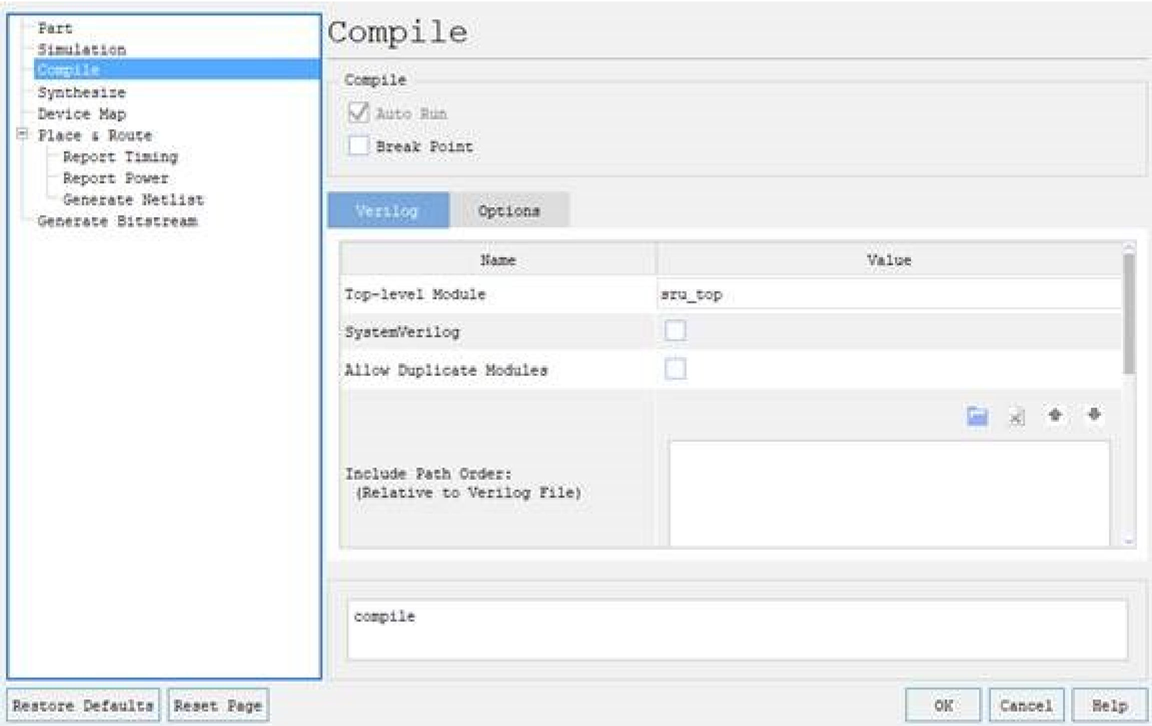


Figure 2-91 option configuration window

2.12 Reporting system

The software provides a relatively complete reporting mechanism: As shown in the figure below, the Report Summary of the reporting system is shown in the figure . Report Summary displays commonly used and important information first on the home page. The report system classifies the information generated by the software and provides related links in Report Summary .

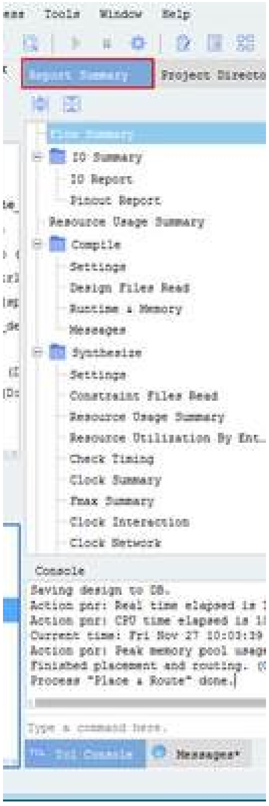


Figure 2-92 Report Report Summary

Synthesize Report: The post-synthesis report mainly introduces the device resource information used in the synthesis process.

Device Map Report : Device Mapping Report, information about the main device mapping.

Place & Route Report: Placement and routing report, mainly device resources used for placement and routing and time information for placement and routing.

Report Timing Report: Timing report after placement and routing, which mainly introduces timing information related to placement and routing.

Report Power Report: Power consumption report after layout and routing, which mainly introduces power consumption information related to layout and routing.

Generate Bitstream Report: The bitstream report mainly introduces the information related to the bitstream.

After the operation is completed, you can click the links to open the corresponding reports for the important reports described above. In addition to the reports that can be opened by clicking the links, the software also provides reports described in files. These report files are placed in the implementation path of the software.

After the modified design file is saved, the report generated by the previous run can still be read in the Report Summary of the PDS interface. After the compilation is restarted, the report generated by the previous run will be grayed out and cannot be read.

The "Project Location" link under the Flow Summary is used to open the file browser of the directory where the project file is located. When opening the PDS project, the Project Directory list on the right side of the Report Summary will be opened by default as shown below. Double-click the corresponding file in the list to open the file in the text editor of PDS .



Figure 2-93 "Project Location" link

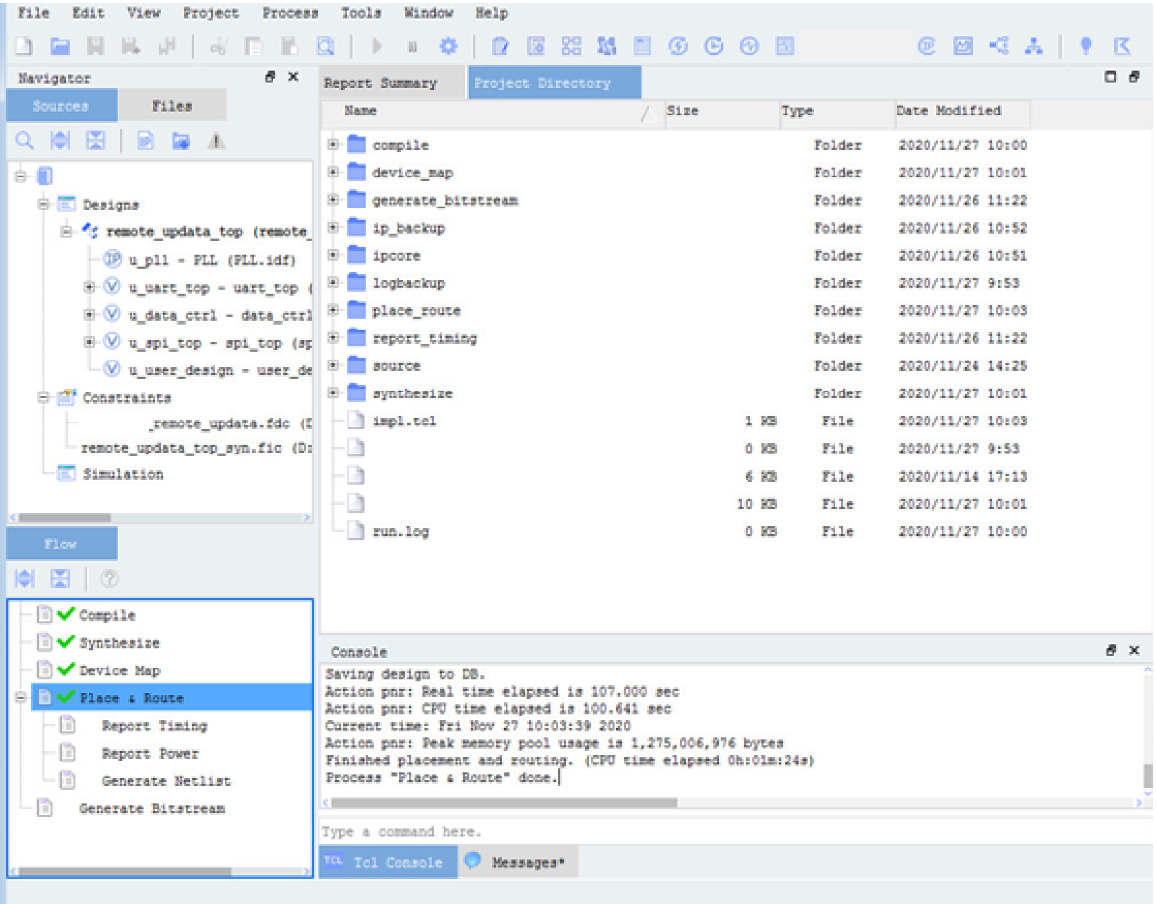


Figure 2-94 "Project Directory" interface

2.13 Text editor

The software provides the default text editing function, as shown in the figure below.

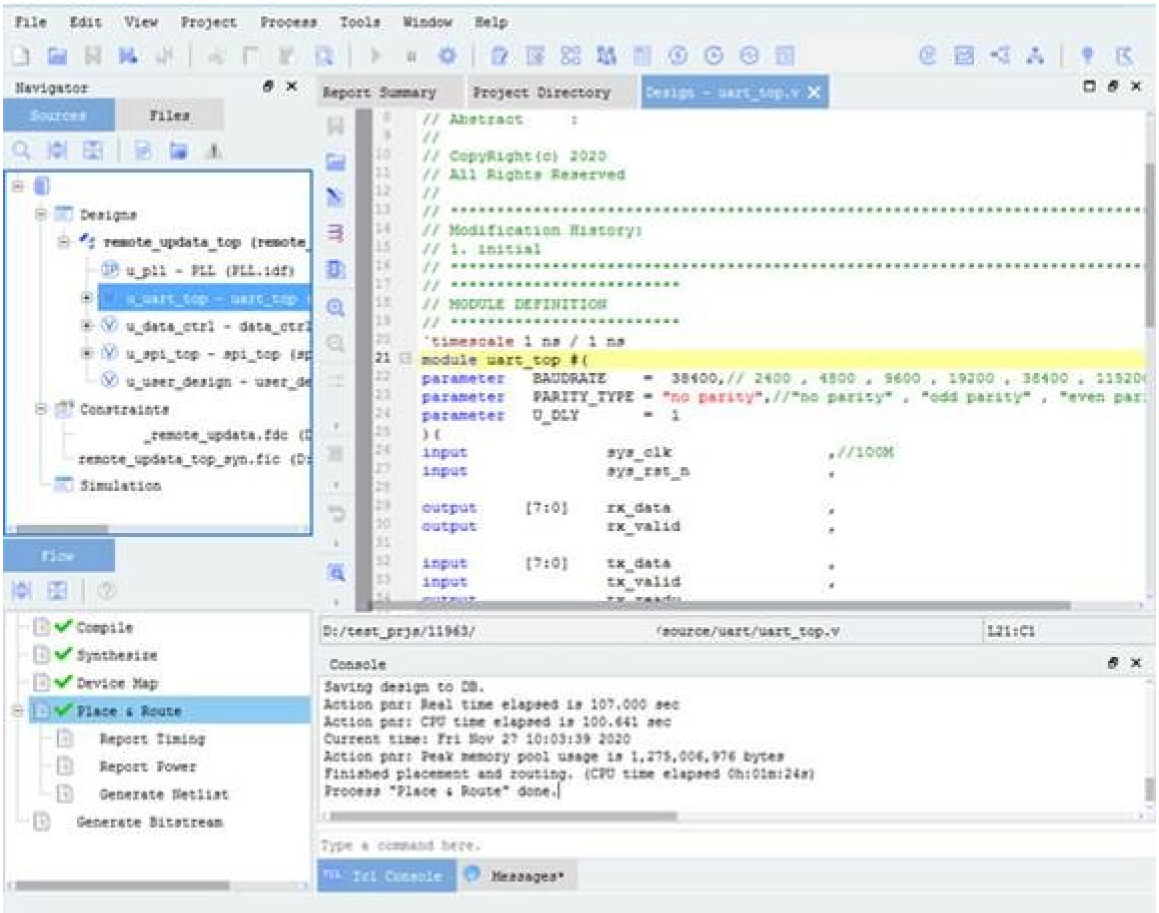


Figure 2-95 The default text editing tool provided by software

Some commonly used editing operations are provided in the left toolbar in the figure above.

Save : Save the file.

Open Containing Folder : Open the directory where the file is located; click the toolbar button , you can open the directory where the file is located.

Read Only : the text is read-only; click the toolbar button , you can activate the read only mode. After activation, you cannot edit the text. Click this button again in the read only mode to cancel the read only mode.

No Wrap : beyond the newline; by default, if you do not enter a newline, the editor will not display the newline, click the toolbar button , it will automatically wrap and display when it exceeds the editing area.

Column Selection Model : Enter column selection and column editing mode.

Zoom In : zoom in; click the toolbar button or use the shortcut key Ctrl+ mouse wheel to scroll up to zoom in on the text font.

Zoom Out : Zoom out; click the toolbar button or use the shortcut key Ctrl+ mouse wheel to scroll down to zoom out the text font.

Increase Indent : Indent the text to the right; select a line in the text, click the button to indent the text to the right, which is equivalent to the Tab key.

Decrease Indent : Indent the text to the left; select a line in the text, click the button to indent the text to the left.

Comment Line : comment text; select a line in the text, click the button in the toolbar or use the shortcut key Alt+C to comment the line.

Uncomment Line : Uncomment the line; select the commented line in the text, click the button or use the shortcut key Shift+Alt+C to cancel the line comment.

Comment Selection : block comment; select a block of content in the text and click (Comment Selection) in the toolbar to add /* */ comments to the selected content.

Uncomment Selection : Uncomment the block ; select the block with /* */ comment, click (Uncomment Selection) in the toolbar, and the /* */ comment of the selected part will be deleted .

Undo : Undo the modification; click on the toolbar button to undo the last modification operation.

Redo : Redo modification; click in the tool bar button to restore the last modification operation.

Find and Replace : Find and replace; click the button in the toolbar or use the shortcut key Ctrl+R to pop up the Find and Replace dialog box to find and replace the text. Enter the searched name and the replaced name as shown in the figure below , click the Replace button to replace one by one, click Replace All to replace all top with out , select Replace All , and a prompt box will pop up to display the replacement location and result after the replacement is completed. Search criteria can be set through the Match Whole Word , Case Sensitive and Wildcard Character (wildcard matching) tabs.

Line Search : Line number search; click the button in the dialog box or use the shortcut key Ctrl+G to pop up the following dialog box to enter the line number, click OK to jump to the corresponding line, and highlight it.

Shortcut key CTRL+D : Copy the content of the line where the cursor is located, and paste it in a new line.

Shortcut key CTRL+L : Cut the content of the line where the cursor is located.

Bookmark function: Left-click on the gray area on the left side of the editor to set a bookmark, which is convenient for switching positions back and forth.

Folding function: For files in verilog format, it supports folding and unfolding in units of modules.

Bracket matching: The editor supports the matching of "(", " [", " { ", that is, if the mouse selects the attachment of the above brackets in the editor, the editor will automatically identify the files between the corresponding brackets.

Modification mark: The editor supports marking the modification traces of the text, that is, if the text has been modified, a red mark will be displayed on the left side of the editor, and it will turn into a green mark after saving.

In addition to the default text editing tools provided by the software, third-party text editing functions can be specified through Preferences under the Edit menu, as shown in the figure below.

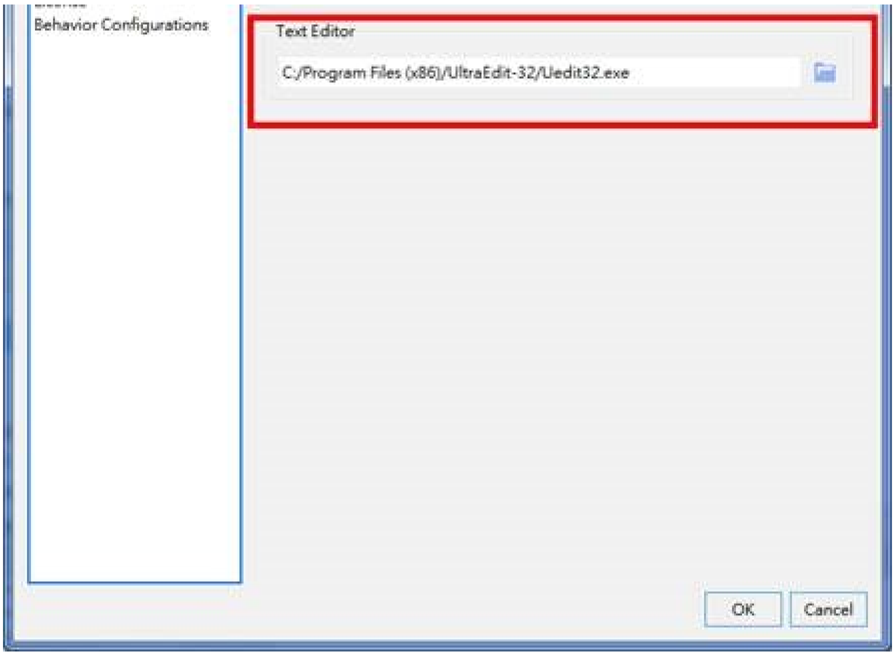


Figure 2-96 Specify text editing tools

As shown in the figure above, Ultra Editor is specified as a text editing tool, so that the user will use UE to open and edit the file next time .

3 Development Process

Through the introduction of the first two chapters, you can have a basic understanding of the PDS software, and then use a simple example to develop and demonstrate the software development process.

Pango Design Suite software mainly includes seven steps:

1. New Project (new project);
2. Add Design/Constraints (add design and constraints);
3. Compile (compile);
4. Synthesize ;
5. Device Map (mapping);
6. Place & Route (layout and routing);
7. Design Editor (view placement and routing and timing analysis results, and manual placement and routing);
8. Generate Bitstream (configuration bitstream).

The following uses a simple example to illustrate the development process of Pango Design Suite, how to use Pango Design Suite software to generate configuration bit stream files. Since steps 1 and 2 have been introduced in the previous chapters, here we start with step 3 Compile .

Take add.v as an example, and explain the timing constraints and physical constraints on the design as an example. In the example, choose C:\pango\PDS_2021.3\example\add\add.v . There is also an add.sdc (timing constraints file) and add.vm in this folder .

Taking the device PGL50H under the Logos series as an example to illustrate the timing constraints and physical constraints on the design.

Note : 1. The basic settings in the example generally adopt the default situation;

2. All configuration options in the instance use the default settings.

3. ADS is used as the synthesis tool in the example; the synthesis tools supported by PDS include ADS and Synplify_Pro , and related documents can be found in 4.1 ADS and 4.2 Synplify_Pro in the relevant plug-ins in Chapter 4 of this document .

3.1 Compile

Compile_settings are introduced as follows: Compile compiles the user's verilog design code into an RTL netlist.

Compile on the main interface, and the right-click menu will pop up as shown in the figure below:



Figure 3-1 Compile right-click menu

Project Setting in the right-click menu, and the following interface will pop up:

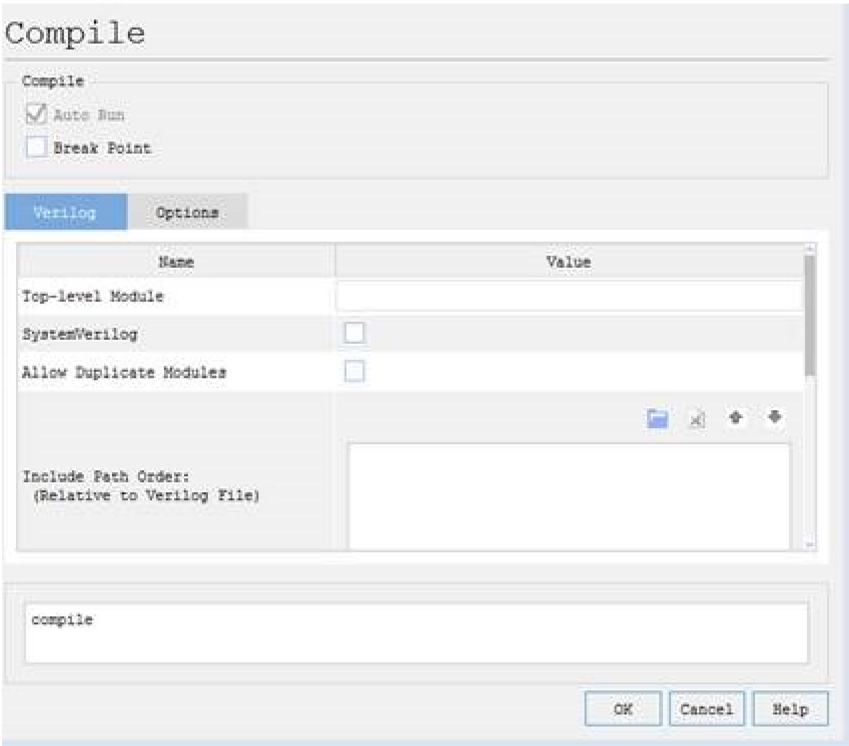


Figure 3-2 Compile option settings

For details about the configuration options of Compile , please refer to Section 3 of Chapter 2 of "ADS_Synthesis_User_Guide " .

After the setting is complete, click Run in the right-click menu to run Compile , and the result is shown in the figure below:

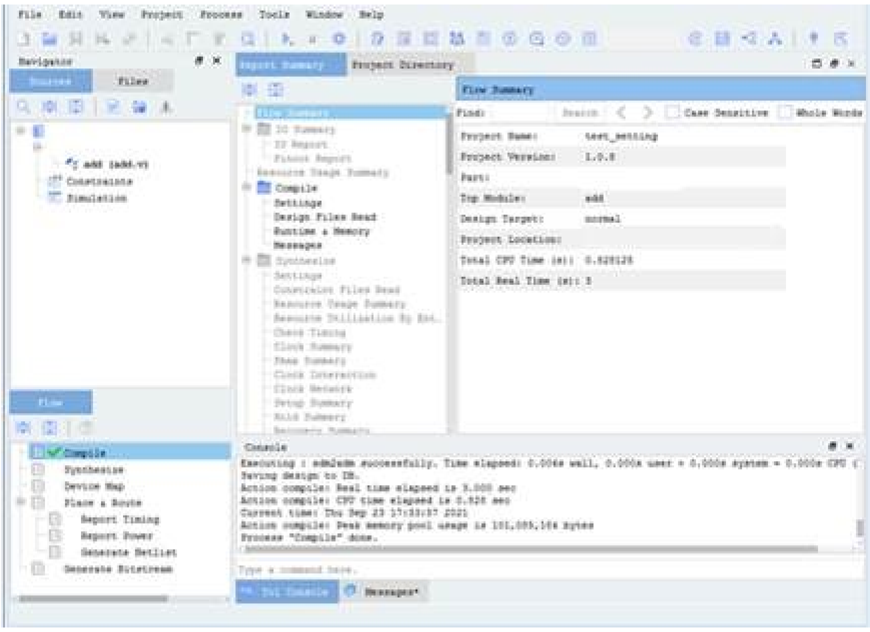


Figure 3-3 Compile result interface

3.2 Synthesize

3.2.1 ADS

Synthesize_settings are introduced as follows: The Synthesize stage is based on the DB of Compile , and the technology netlist is generated after mapping and optimization .

Synthesize on the main interface, and the right-click menu will pop up as shown in the figure below:

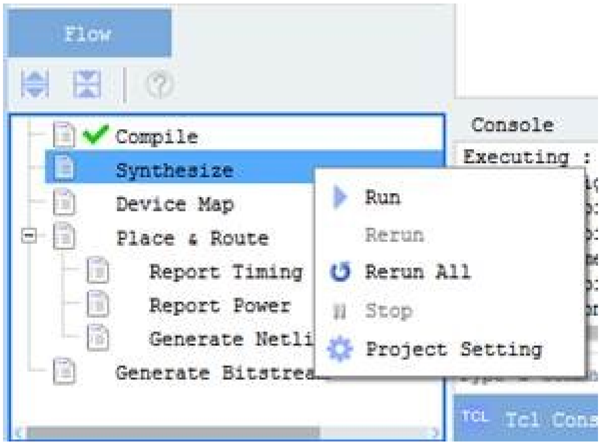


Figure 3-4 Synthesize right-click menu

Project Setting in the right-click menu, and the following interface will pop up:

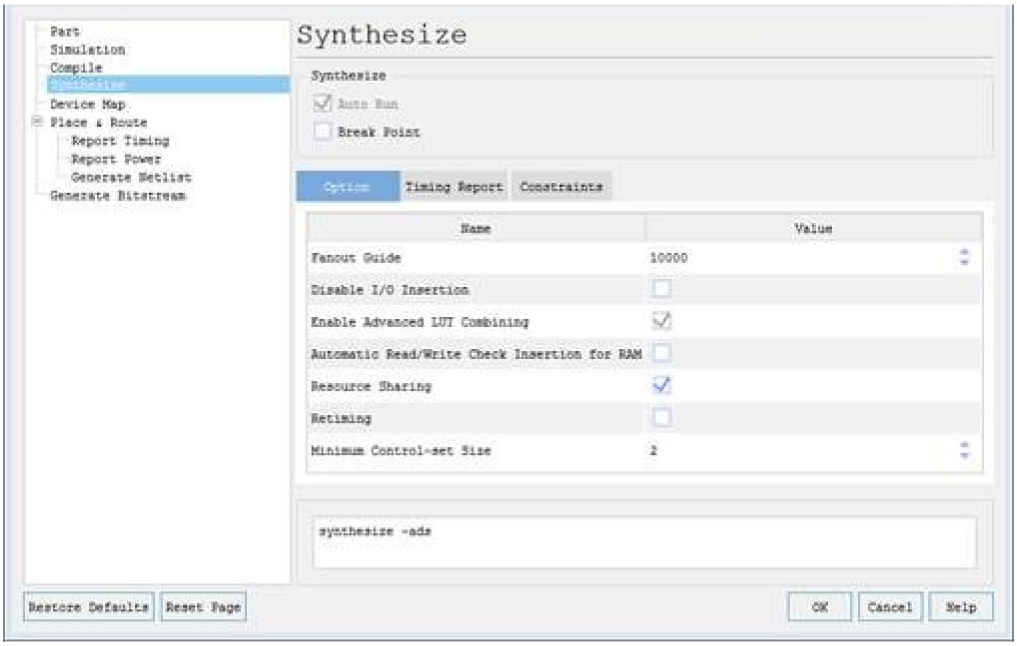


Figure 3-5 Synthesize option settings

The configuration options of Synthesize can be found in Section 3 , Chapter 2 of " ADS_Synthesis_User_Guide " .

After the setting is complete, click Run in the right-click menu to run Synthesize , and the result is shown in the figure below:

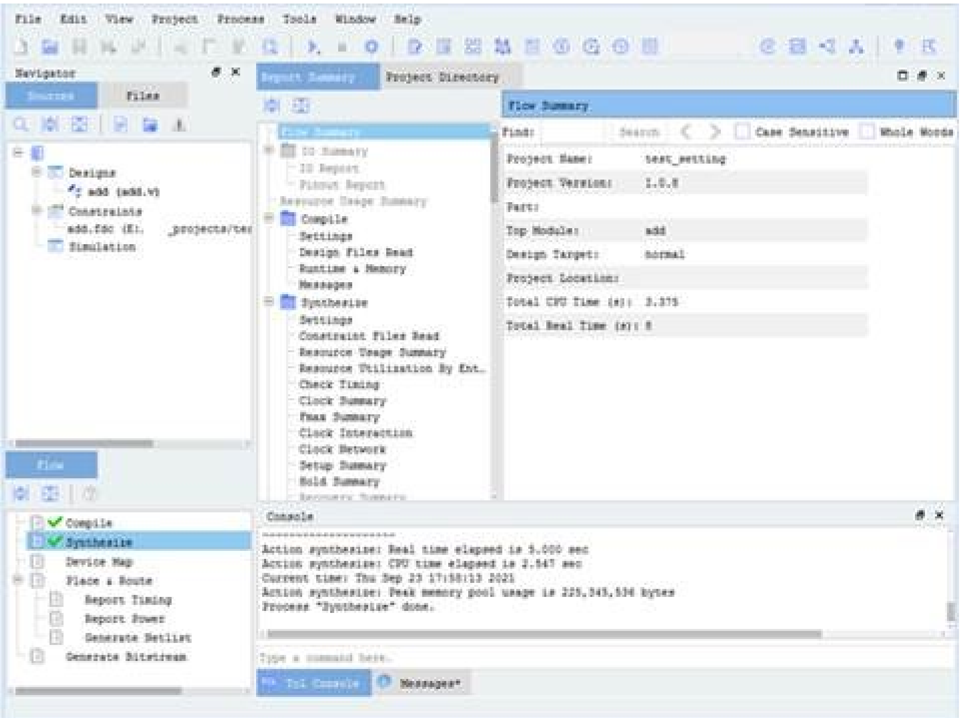


Figure 3-6 Run the Synthesize result interface

From the figure above, you can see that the link to the Synthesize -related Report in the Flow Summary can be clicked to open. Click Synthesize with the mouse to see the text report of synthesize , as shown in the figure below.

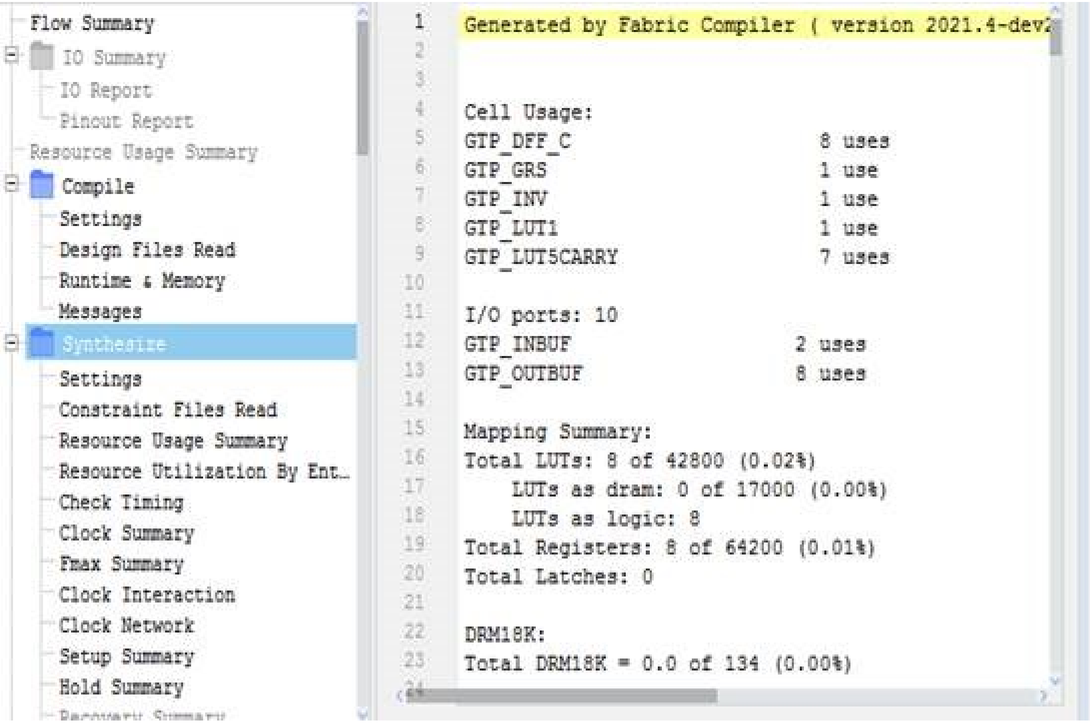


Figure 3-7 Synthesize text report

You can also right-click the position shown in the figure below and click Open Report to open the report shown in the figure above. In addition, as shown in the figure below, right-clicking can also open the folder where the report is located by clicking Open Containing Folder (for subsequent steps, it is consistent with the synthesizesize , and clicking the item with the same name as the step in Flow in the flow summary can open the text report, and the report can be opened when right-clicking location folder and text report).

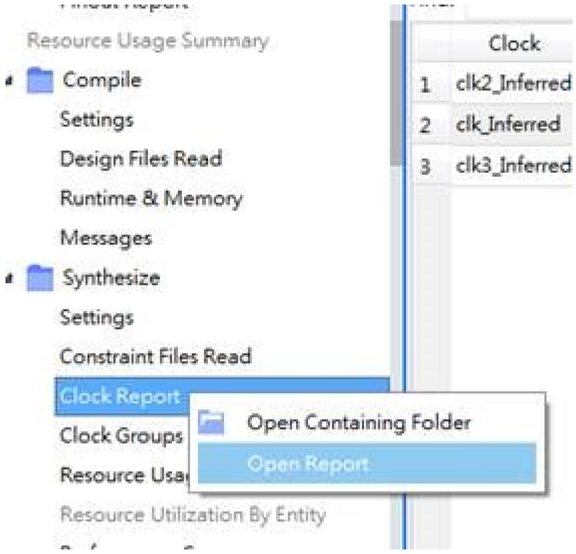


Figure 3-8 Right-click menu in report area

Click the Performance Summary to see the following interface (to view other reports similar, just click the corresponding item) :

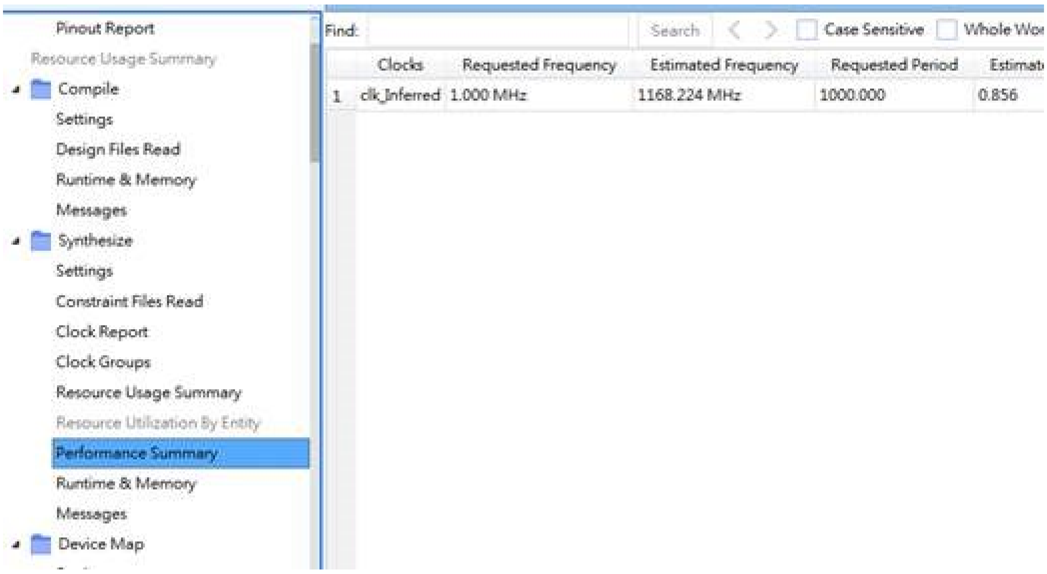


Figure 3-9 Synthesize Report

In the figure above, there is a search bar below the Performance Summary . You can enter the characters to be searched in the text input box, and click the Search button behind to perform the search operation. If there are multiple search results, the following "previous" or "next" search results will be highlighted, click " previous " to jump to the previous search result, and click " next " to jump to the next search result. When searching, you can also choose whether to match case, or match whole words. Right-click in the table report, you can see the following right-click menu.

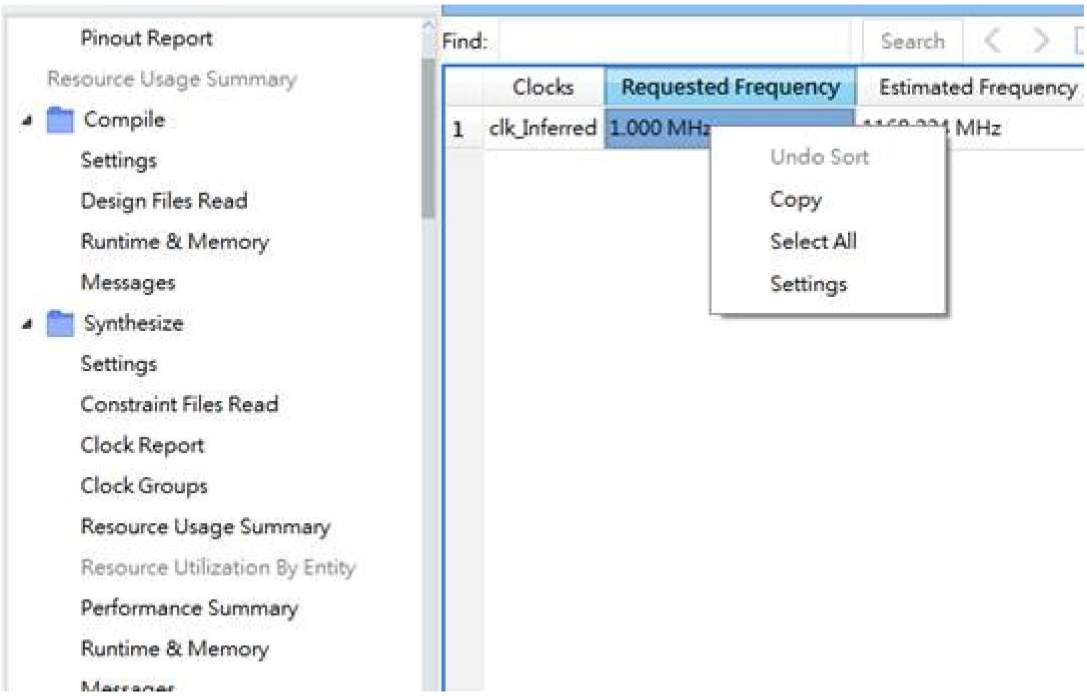


Figure 3-10 Form right-click menu

Click the header of each column (such as the Staring Clock in the figure above) to sort, and Undo Sort can restore the order of the table content when the report was generated. When there is selected content in the table, the selected content can be copied by Copy . Select All can select the entire table. The row height of table data can be set in Settings , as shown in the figure below

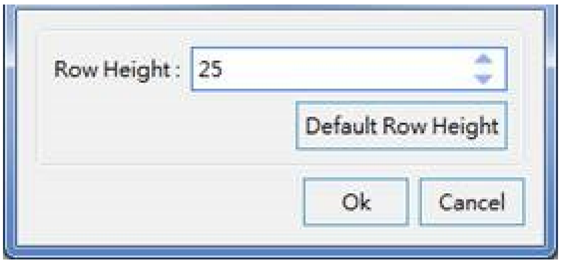


Figure 3-11 Set table row height interface

Table row height defaults to 25 pixel .

3.2.2 Synplify_Pro

The user's verilog or VHDL design code can also be synthesized using a third-party synthesis tool. The synthesis is based on the library of the target FPGA , and the generated VM file is used as the design input of Pango Design Suite . The VM file format generated by third-party synthesis tools is verilog .

The former simulation library directory is $InstallDir\arch\vendor\pango\verilog\simulation , such as: C:\pango\PDS_2021.3\arch\vendor\pango\verilog\simulation .

Synthesize in the lower figure of the main interface, and the right-click menu as shown in the figure below will pop up

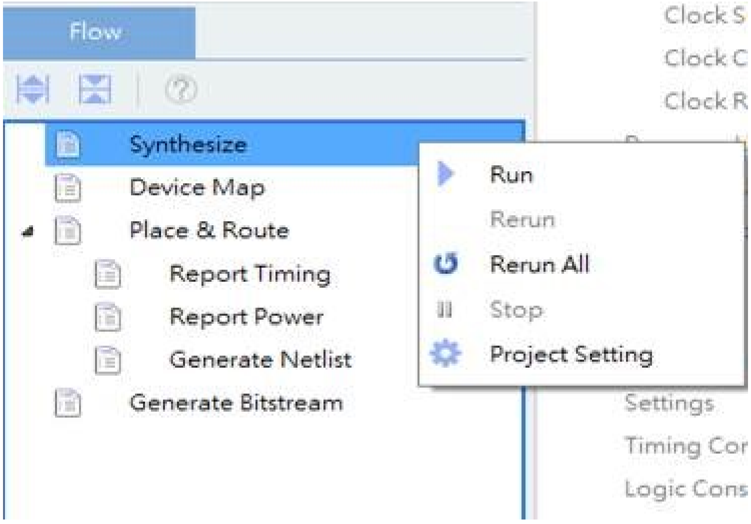


Figure 3-12 Synthesize right-click menu

Project Setting in the right-click menu, and the following interface will pop up.

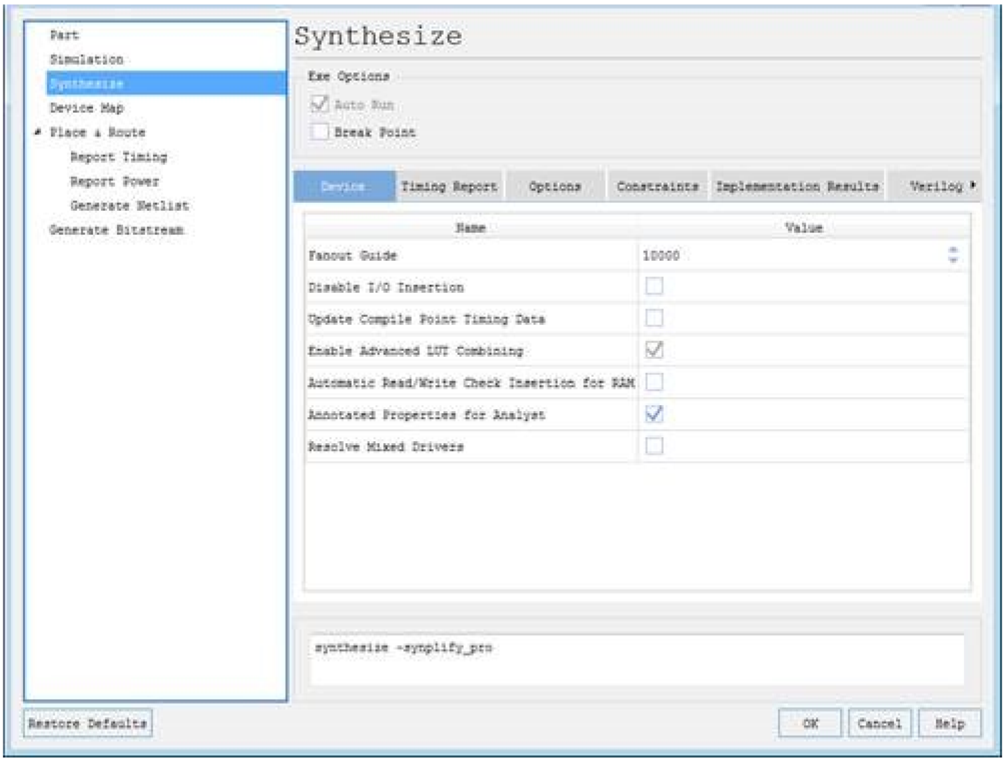


Figure 3-13 Synthesize-device tab configuration option interface

The following options are involved in the above figure (the detailed description of the options shown in the above figure can be found in the Pango Device Mapping Options section on page 319 of the fpga_reference.pdf document in the subdirectory syn/doc in the installation directory) :

Fanout Guide : Sets a guideline for the fanout limit. The default is 10000. For tips on setting and using fanout limits, see Setting Fanout Limits and Controlling Buffering and Replication.

Disable I/O Insertion : When enabled, it prevents automatic I/O insertion during synthesis. By default, it is disabled.

Update Compile Point Timing Data : Determines whether changes to a locked compile point force its parents to be remapped and updated with the new timing model of the child. See Compile Point Basics, for details.

Enable Advanced LUT Combining : Prepare netlist for advanced LUT combining.

Automatic Read/Write Check Insertion for RAM : Lets the synthesis tool insert bypass logic around the RAM to prevent a simulation mismatch between the RTL and post-synthesis simulations. The synthesis software globally inserts bypass logic around the RAM that reads and writes to the same address simultaneously. Disable this option, when you cannot simultaneously read and write to the same RAM location and want to minimize overhead logic.

Annotated Properties for Analyst : Annotates the design with properties after the design is compiled. You can view these properties in the schematic views

Resolve Mixed Drivers : When a net is driven by a VCC or GND and active drivers, enable this option to connect the net to the VCC or GND driver.

Click the timing Report tab in the figure above, and the following interface appears:

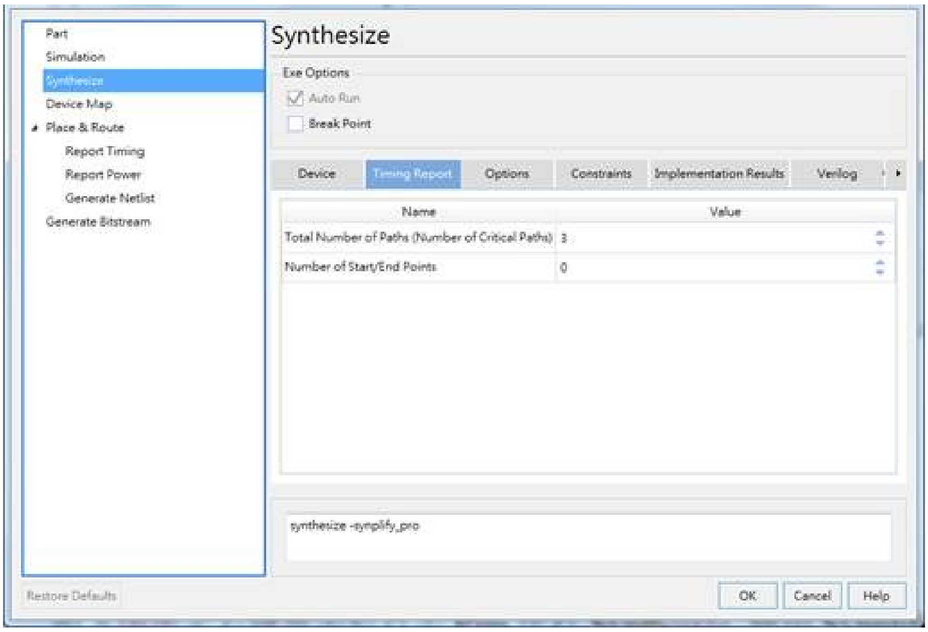


Figure 3-14 synthesize-Timing Report tab configuration option interface

The above figure involves the following comprehensive options (the detailed description of the options shown in the above figure can be found in the Timing ReportPanel section on page 316 of the fpga_command_reference.pdf document in the subdirectory syn/doc in the installation directory) :

Total Number of Paths (Number of Critical Paths) : Set the number of critical paths for the software to report.

Number of Start/End Points : Specify the number of start and end points to see reported in the critical path sections .

Click the Options tab in the above figure, and the following interface appears

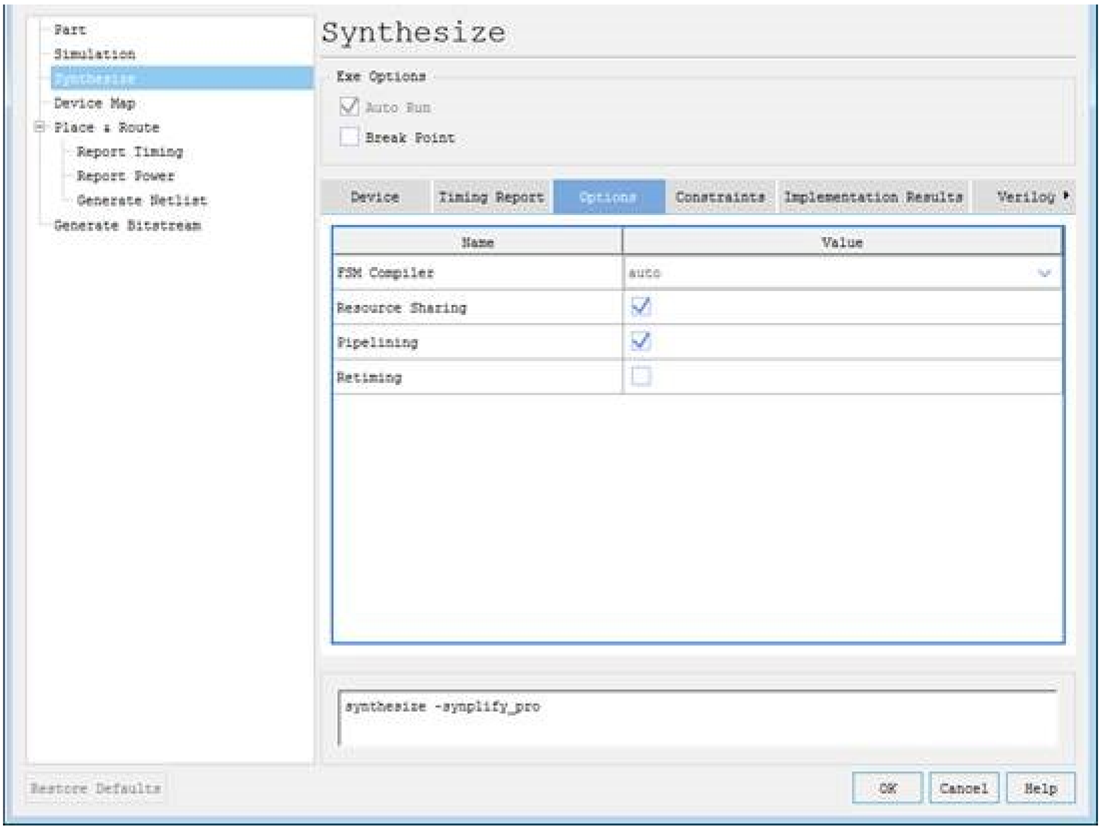


Figure 3-15 synthesize-Options tab configuration option interface

The comprehensive options involved in the above figure are as follows (the detailed description of the options shown in the above figure can be found in the Options Panel section on page 311 of the fpga_command_reference.pdf document in the subdirectory syn/doc in the installation directory) :

FSM Compiler : Determines whether the FSM Compiler is run

Pipelining : Runs designs at a faster frequency by moving registers after the multiplier or ROM into the multiplier or ROM

Resource Sharing : Determines whether you optimize area by sharing resources. When enabled, this optimization technique runs during the compilation stage of synthesis. Even if it is disabled, the mapper can still flatten the netlist and re-optimize adders, multipliers as needed to improve timing, because this setting does not affect the mapper

Retiming : Determines whether the tool moves storage devices across computational elements to improve timing performance in sequential circuits. Note that the tool might retime registers associated with RAMs, DSPs, and generated clocks, regardless of the Retiming setting.

Click the constraints tab in the above figure, and the following interface appears

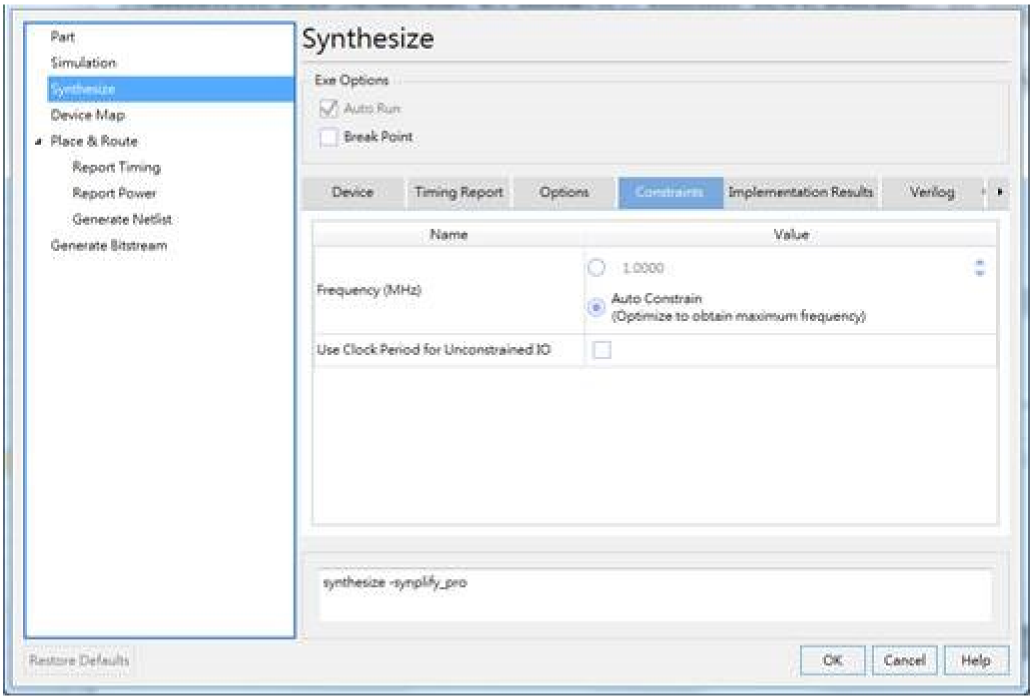


Figure 3-16 synthesize-Constraints tab configuration option interface

The comprehensive options involved in the above figure are as follows (the detailed description of the options shown in the above figure can be found in the Constrain s Panel section on page 313 of the fpga_command_reference.pdf document in the subdirectory syn/doc in the installation directory) :

Frequency (MHz): Sets the default global frequency. You can either set the global frequency here or in the Project view. To override the default you set here, set individual clock constraints from the SCOPE interface.

Auto Constrain : When enabled and no clocks are defined, the software automatically constrains the design to achieve the best possible timing. It does this by reducing periods of each individual clock and the timing of any timed I/O paths in successive steps.

Use clock period for unconstrained IO : Determines whether default constraints are used for I/O ports that do not have user-defined constraints. When disabled, only define_input_delay ordefine_output_delay constraints are considered during W synthesis shen or forward-annotated wares is enabled after . considers any explicit define_input_delay ordefine_output_delay constraints. In addition, for all ports without explicit constraints, it uses constraints based on the clock period of the attached registers. Both the explicit and implicit constraints are used for synthesis and forward- disabled) for new designs.

Click the Implementation Results tab in the above figure, and the following interface appears:

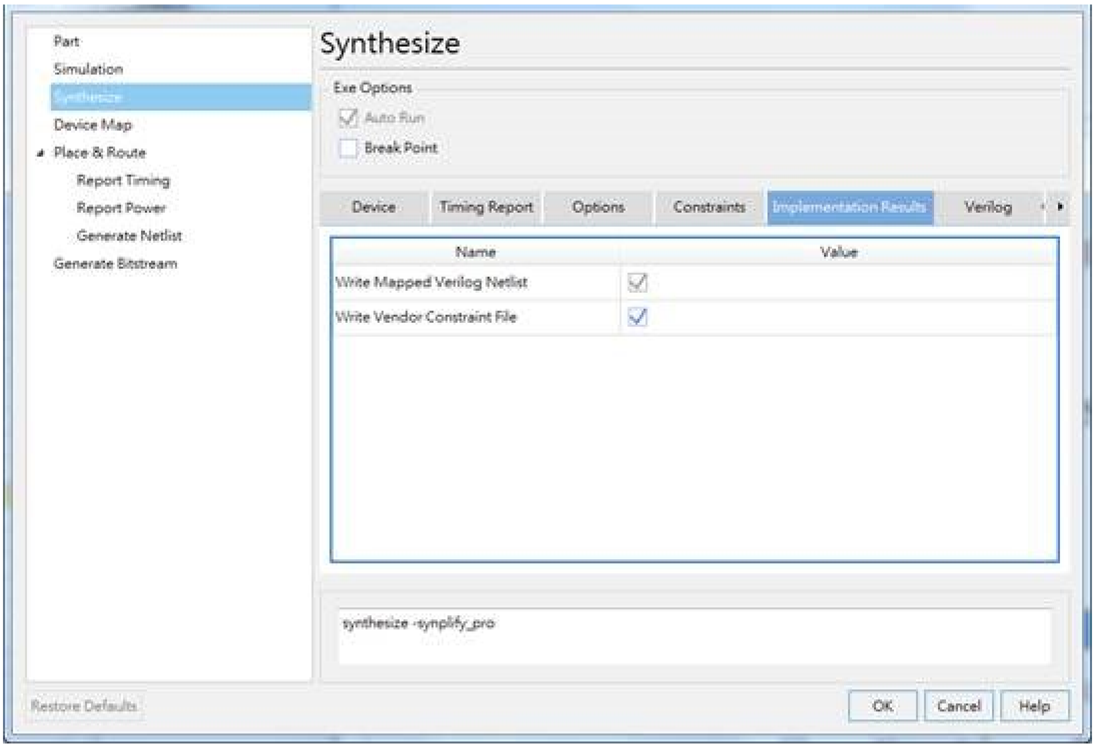


Figure 3-17 synthesis-Implementation Results tab configuration option interface

The following comprehensive options are involved in the above figure (the detailed description of the options shown in the above figure can be found in the Implementation Results Panel section on page 314 of the fpga_command_reference.pdf document in the subdirectory syn/doc in the installation directory) :

Write Mapped Verilog Netlist : Generates mapped Verilog or VHDL netlist files.

Write Vendor Constraint File : Generates a vendor-specific constraint file for forward annotation.

Click the Verilog tab in the above figure, and the following interface appears:

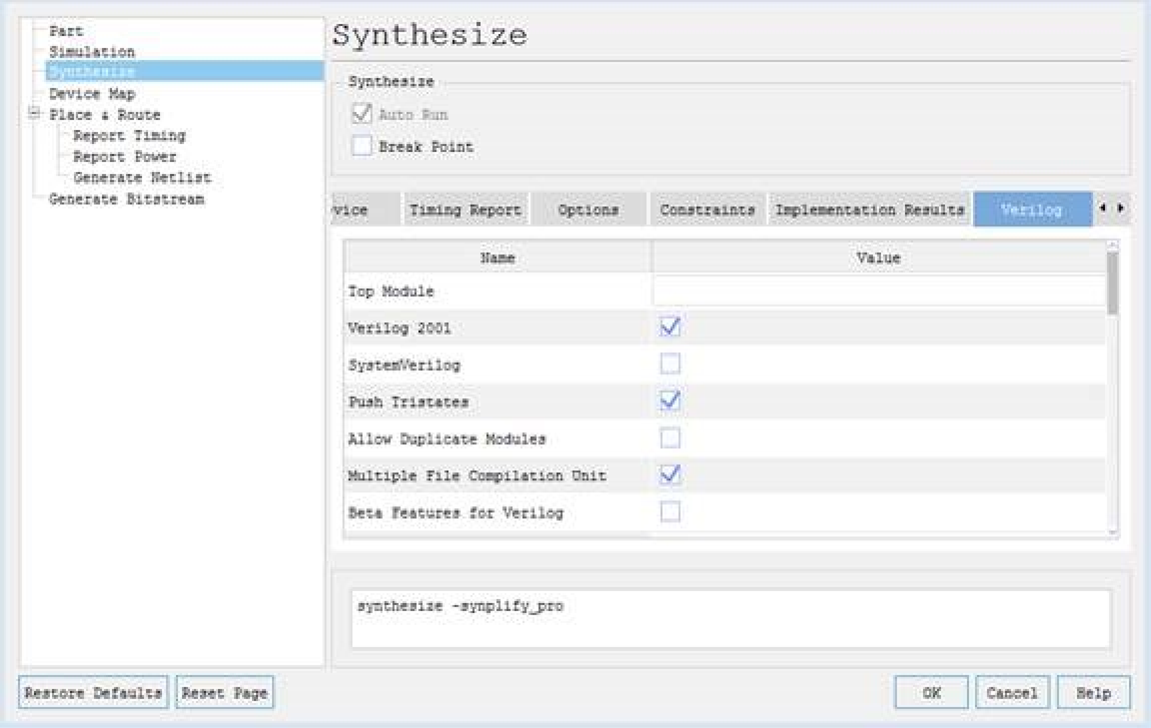


Figure 3-18 synthesize-Verilog tab configuration option interface

The following comprehensive options are involved in the above figure (the detailed description of the options shown in the above figure can be found in the Verilog Panel section on page 320 of the fpga_command_reference.pdf document in the subdirectory syn/doc in the installation directory) :

Top Module : The name of the top-level module of your design.

Verilog 2001 : When enabled, the default Verilog standard for the project is Verilog 2001. When both Verilog 2001 and SystemVerilog are disabled, the default standard is Verilog 95.

SystemVerilog : When enabled, the default Verilog standard for the project is SystemVerilog which is the default standard for all new projects. Enabling SystemVerilog automatically enablesVerilog 2001.

Push Tristates : When enabled (default), tristates are pushed across process/block boundaries.

Allow Duplicate Modules : Allows the use of duplicate modules in your design. When enabled, the last definition of the module is used by the software and any previous definitions are ignored. You should not use duplicate module names in your Verilog design, therefore this option is disabled by default. However, if you need to, you can allow for duplicate modules by enabling this option.

Multiple File Compilation Unit : When enabled (the default), the Verilog compiler uses the compilation unit for modules defined in multiple files.

Beta Features for Verilog : Enables use of any Verilog beta features included in the release.

Loop Limit :Allows you to override the default compiler loop limit value of 2000 in the RTL.

Include Path Order (Relative to Verilog File) : Specifies the search paths for the include commands in the Verilog design files of your project. Use the buttons in the upper right corner of the box to add, delete, or reorder the paths. The include paths are relative.

Library Directories orFiles : Specifies all the paths to the directories which contain the Verilog library files to be included in your design for the project.

Library Extensions (space separated) : Adds library extensions to Verilog library files included in your design for the project and searches the directory paths you specified that contain these Verilog library files.

Generics : Shows generics extracted with Extract Generic Constants. You can override the default and set a new value for the generic constant. The value is valid for the current implementation.

Compiler Directives : Provides an interface where you can enter compiler directives that you would normally enter in the code with 'ifdef and 'define statements.

Click the VHDL tab in the above figure, and the following interface appears

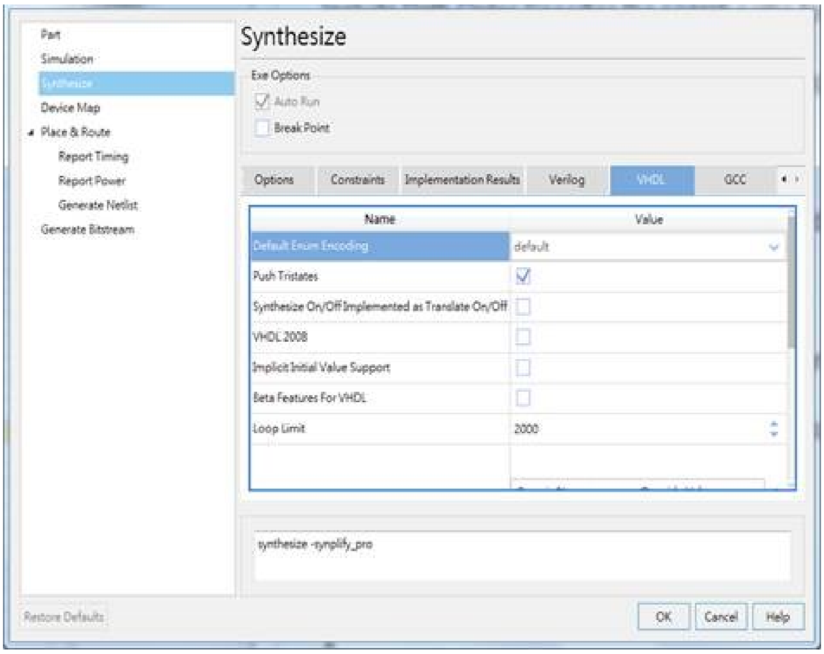


Figure 3 -19 synthesize-VHDL tab configuration option interface

The above figure involves the following comprehensive options (the detailed description of the options shown in the above figure can be found in the VHDL Panel section on page 317 of the fpga_command_reference.pdf document in the subdirectory syn/doc in the installation directory) :

Default Enum Encoding : The default enumeration encoding to use. This is only for enumerated types; the FSM compiler automatically determines the state-machine encoding, or you can specify the encoding using the syn_encoding attribute.

Push Tristates : When enabled (default), tristates are pushed across process/block boundaries.

Synthesis On/Off Implemented as Translate On/Off : When enabled, the software ignores any VHDL code between synthesis_on and synthesis_off directives. It treats these third-party directives like translate_on/translate_off directives (see translate_off de/translate_on.

VHDL 2008 : When enabled, allows you to use VHDL 2008 language standards.

VHDL 2019 : When enabled, allows you to implement VHDL 2019 conditional analysis identifiers and values.

Implicit Initial Value Support : When enabled, the compiler passes init values through a syn_init property to the mapper.

Beta Features for VHDL: Enables use of any VHDL beta features included in the release.

Loop Limit : Allows you to override the default compiler loop limit value of 2000 in the RTL. You can apply loop limits using the Verilog loop_limit or the VHDL syn_looplimit directive.

Generics : Shows generics extracted with Extract Generic Constants. You can override the default and set a new value for the generic constant. The value is valid for the current implementation.

Click the GCC tab in the above figure, and the following interface appears:

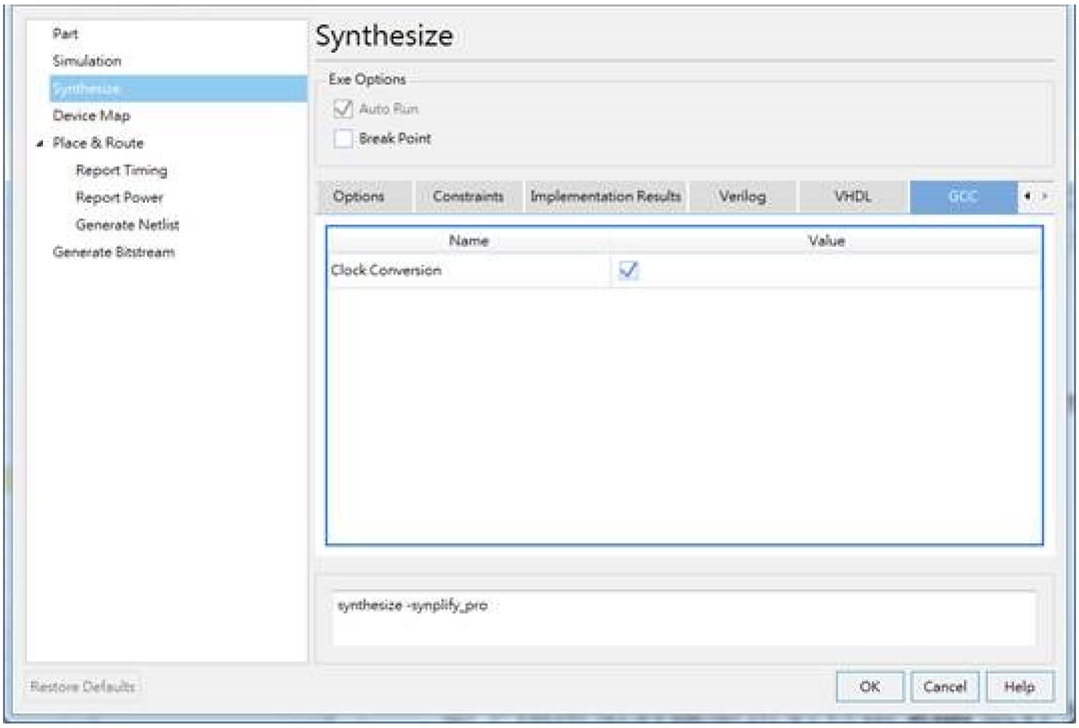


Figure 3-20 synthesize-GCC tab configuration option interface

The above figure involves the following comprehensive options (the detailed description of the options shown in the above figure can be found in the GCC Panel section on page 334 of the fpga_command_reference.pdf document in the subdirectory syn/doc in the installation directory) :

Clock Conversion : Performs gated and generated clock optimization when enabled.

After clicking, right-click Run to run Synthesize as shown in the figure below , and use the Synplify Pro synthesis tool to compile the .v file to generate a .vm netlist file.

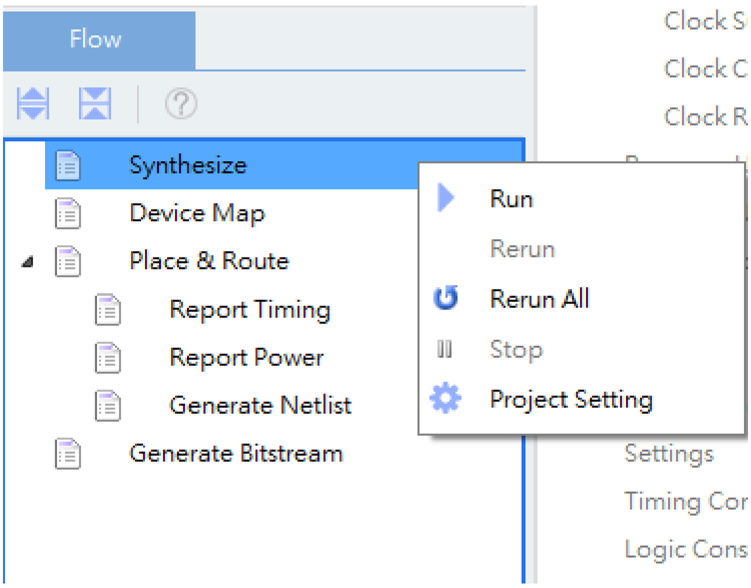


Figure 3-21 Run Synthesize

After completing the above operations, you will see the interface as shown in the figure below

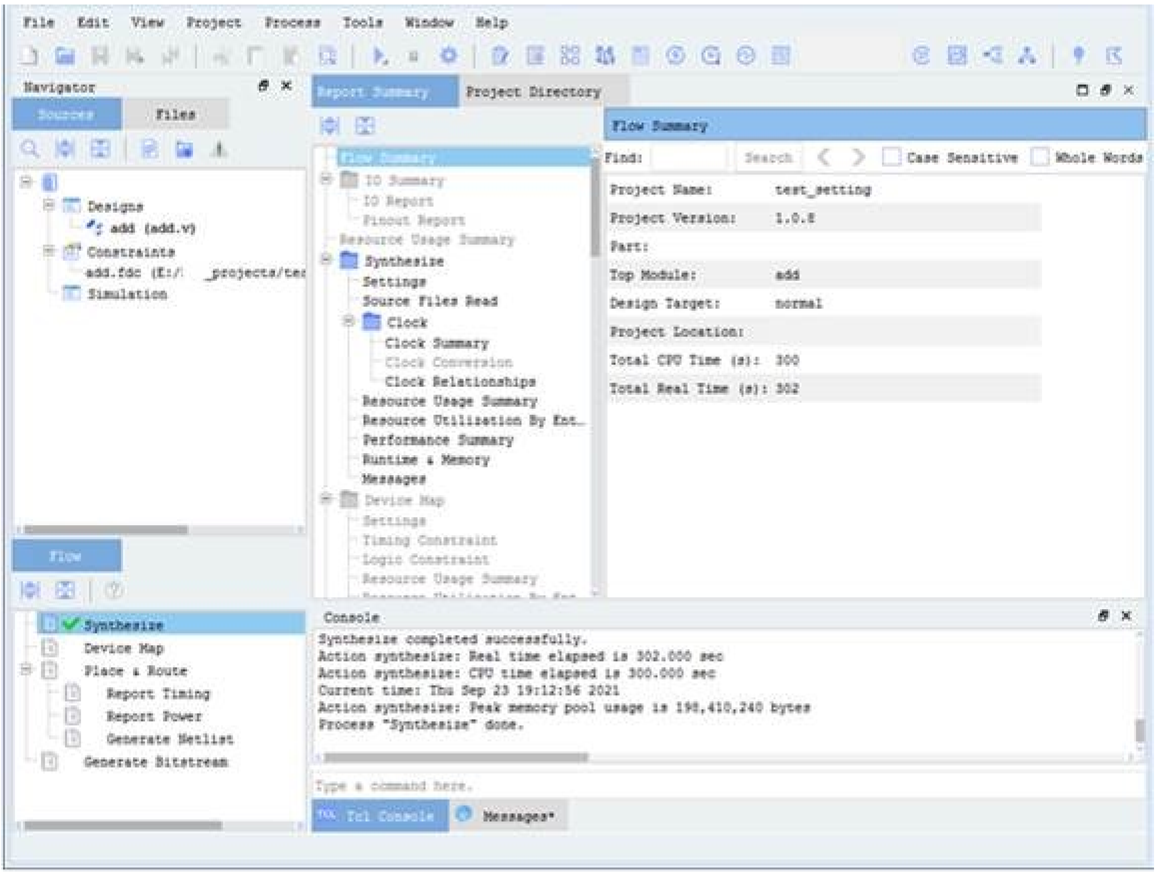


Figure 3-22 Software interface after running Synthesize

3.3 Device Map

Device_Map_settings are introduced as follows: The main function of Map mapping is to map the design to specific models of subunits (LUT , FF , Carry , etc.).

Device Map option settings As shown below:

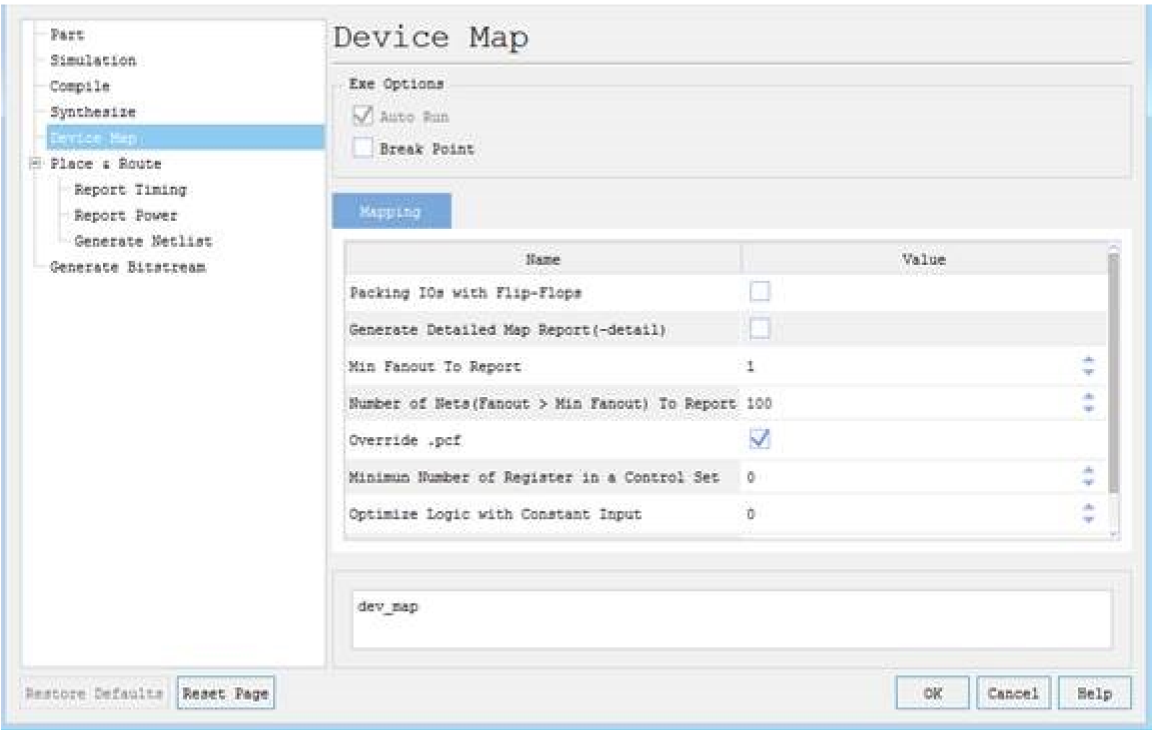


Figure 3-23 Device Map option settings

Device Map configuration options:

【 Packing IOs with Flip-Flops 】 Set whether to add when mapping IO Flip-Flops . Indicates whether to pack the FFs directly connected to the IO port into the corresponding IO port. The input and output modes of this IO port can be input , output , inout . By default, this option is not selected, that is, FF is not together with IO Pack .

【 Generate Detailed Map Report(-detail) 】 Set whether to print the resource usage of each module instance in the report file of the map . This option is not selected by default.

【 Min Fanout To Report 】 Set the minimum number of net fanouts printed in the map report . The default value is 1 .

【 Number of Nets(Fanout > Min Fanout) To Report 】 Set the number of nets to be printed in the map report, and the fanout of the printed net must be greater than the minimum fanout setting value. The default value is 100 .

【 Override.pcf 】 This item is used to set whether to overwrite the existing pcf when the pcf constraint information generated by the user constraint file (fdc/lcf) is inconsistent with the existing pcf file constraint information . If the value is true , pcf will be overwritten automatically when device map is executed ; if the value is false , pcf will not be overwritten . This option is selected by default.

[Enable timing commands commented by Synplify Pro] This item is used to set the enable state, that is , the timing commands marked as comments by the OEM can take effect in the PDS process. This option is not selected by default. (ADS synthesis not supported)

【 Minimum Number of Register in a Control Set 】 It is used to control the minimum number of triggers under the same control set . But when the number of flip-flops is less than the threshold, the gating signal is implemented as a data path with LUT . Control set refers to the clock, enable signal, and RST signal of the flip-flop. Optimizing this control signal can increase resource usage. The default value is 0 .

[Optimize Logic with Constant Input] is mainly used to optimize the input constant logic. Constant logic mainly refers to VCC , GND logic. The optimization operation mainly disconnects or optimizes the original VCC and GND to the optimal state through the inherent characteristics of the circuit. The default value is 0 .

[Remove Duplicated Logic] The main function of this function is to merge some duplicated logic, which belongs to the area optimization option. However, this operation will also affect the copy work in the synthesis stage, which will degrade the timing performance. The default value is 0.

After completing the settings, execute the device map and the result is as follows:

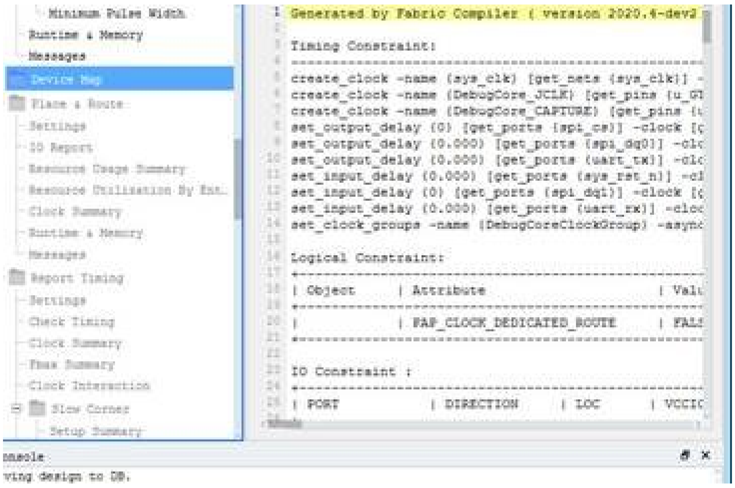
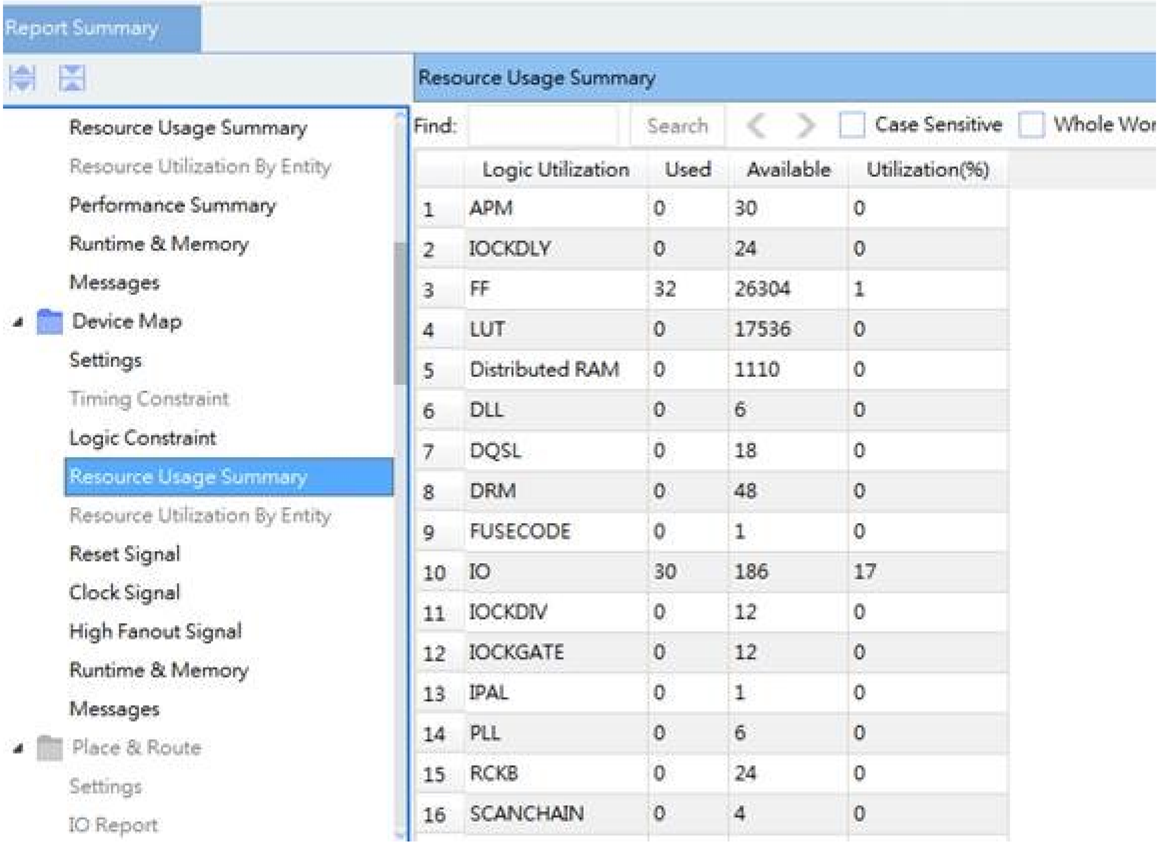


Figure 3-24 Software interface after Device Map

Click Resource Usage Summary , the result is as follows:



	Logic Utilization	Used	Available	Utilization(%)
1	APM	0	30	0
2	IOCKDLY	0	24	0
3	FF	32	26304	1
4	LUT	0	17536	0
5	Distributed RAM	0	1110	0
6	DLL	0	6	0
7	DQSL	0	18	0
8	DRM	0	48	0
9	FUSECODE	0	1	0
10	IO	30	186	17
11	IOCKDIV	0	12	0
12	IOCKGATE	0	12	0
13	IPAL	0	1	0
14	PLL	0	6	0
15	RCKB	0	24	0
16	SCANCHAIN	0	4	0

Figure 3-25 Device Map Resource Usage Summary interface

3.4 Place & Route

3.4.1 Place & Route Settings

Place_Route_settings are introduced as follows: Place & Route (Place & Route) performs actual placement and routing of design modules according to user constraints and physical constraints.

Place & Route are shown in the figure below:

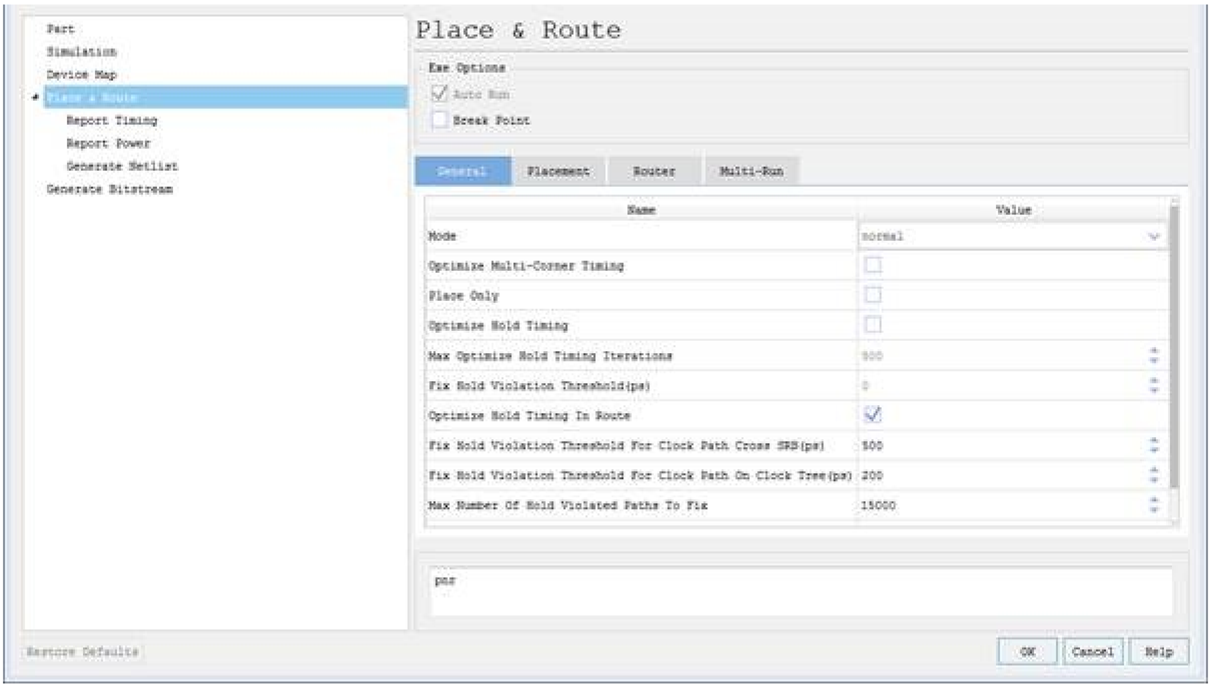


Figure 3-26 Place & Route option settings

Place & Route configuration options:

A. Conventional module:

【 Mode 】 There are three options: fast, normal and performance.

- fast mode - the fastest running speed, the worst performance;
- normal mode - takes into account both performance and speed, can meet the general design requirements;
- performance mode - the best performance, but the longest running time. Defaults to normal.

【 Optimize multi-corner timing 】 Whether to turn on the multi-corner function when repairing the hold violation is only valid after the Optimize Hold Timing is turned on. When enabled, hold fix fixes both slow corner and fast corner hold violations. If not enabled, hold fix fixes fast corner violations by default. This option is not selected by default.

【 Place Only 】 Only layout without routing. This option is not selected by default.

【 Optimize Hold Timing 】 When the design has a hold violation, whether to fix the violation. This option is not selected by default.

【 Max Optimize Hold Timing Iterations 】 When Optimize Hold Timing is checked, this option indicates the maximum number of iterations for repairing violations, and stops repairing Hold violations when the maximum number of iterations is reached. The default value is 500.

【 Fix Hold Violation Threshold(ps) 】 When Optimize Hold Timing is ticked, you can use this option to optimize Hold timing for timing paths whose slack is less than this value, thereby leaving a certain margin for Hold timing (unit: ps). The default value is 0.

【 Optimize Hold Timing In Route 】 When a design has a hold violation, whether to fix the violation during routing. This option is selected by default.

【 Fix Hold Violation Threshold For Clock Path Cross SRB(ps) 】When Optimize Hold Timing In Route is checked, you can use this option to optimize Hold timing for timing paths with slack less than this value, thus leaving a certain margin for Hold timing (unit: ps), This parameter takes effect only when the clock path corresponding to the violation path passes the SRB . If this parameter is set too large, It may be because there are many violations that need to be repaired, and the repair time is long. If this parameter is set too small, there is a risk of hold timing violations. The recommended parameter value setting range is 【0, 1800】 . The default value is 200.

【 Fix Hold Violation Threshold For Clock Path On Clock Tree(ps) 】 When Optimize Hold Timing In Route is ticked, you can use this option to optimize Hold timing for timing paths whose slack is less than this value, thus leaving a certain margin for Hold timing. Amount (unit: ps), this parameter takes effect only when the clock path corresponding to the violation path does not pass the SRB , and the setting interval is 【0 , 200】 . The default value is 100 .

【 Max Number Of Hold Violated Paths To Fix 】When Optimize Hold Timing In Route is checked, you can use this option to limit the number of paths that can be processed in the hold fix process. When the limit is exceeded, hold violation repair will not be performed. Set the interval to 【0, 100000】 . The default value is 15000.

In particular, the function to fix hold violations will report the following warning:

1 . C: Route-2015

1) Trigger scenario:

When the worst hold slack value exceeds 5000 ps , this Critical Warning will be reported , and hold repair will not be performed ;

2) Example:

C: Route-2015:Hold violation is 6000 ps over the critical value of 5000 ps, beyond the critical value will not be repaired. The above warning means that the worst slack value in the project is 6000 ps , exceeding 5000 ps ;

3) Solution:

When reporting C:Route-2015 , the user needs to reconfirm whether the clock planning of the project is reasonable, and the clock exceeds 5000ps . hold is violated. In this case, the user needs to adjust the project according to the actual situation.

2. C: Route - 2037

1) Trigger scenario:

When the number of hold violation paths in the project exceeds the value set by the "Max Number Of Hold Violated Paths To Fix" option, the hold timing repair process will not be executed,

and this Critical Warning will be reported, and hold repair will not be performed;

2) Example:

C: Route-2037: Number of hold violated paths is 15012, over the limit 15000 and hold violation fix will be stopped, you can change the value of option "Place & Route" -> "Max Number Of Hold Violated Paths To Fix". The above warning indicates that the number of paths with hold violations in the project is 15012 , and the value set in the options is 15000. At this time, hold repair will not be performed ;

3) Solution:

When reporting C:Route-2037 , the user can modify the value in option "Place & Route" -> "Max Number Of Hold Violated Paths To Fix" according to the number of paths indicated in the warning , and then restart the Run place and route.

3. C: STA-3017 and W : Timing-4105

1) Trigger scenario:

when the hold fix switch is turned on, After the hold violation is fixed , if the hold slack on the endpoint does not meet the hold violation threshold set by the user , these two Warnings will be reported (only for the launch clock or capture clock to take the SRB path) ; when the hold fix is closed, the These two Warnings ; C: STA-3017 is used to prompt the user to have the number of paths that do not satisfy the margin , W: Timing-4105: the endpoint , clock and corresponding paths of the path with the worst hold that are used to prompt the user not to satisfy the margin slack ;

2) Example:

C: STA-3017: There are 10 clock cross SRB paths do not meet the required hold violation threshold (500ps). The above warning indicates that there are 10 clocks crossing SRB paths and the hold margin of the paths do not meet the value set by the user (the default value is 500ps , can be changed)

W:Timing-4105: The worst slack of endpoint t1daau_dp/dsmnbop 【5】/opit_0/D of clock lclkp is -115ps(fast corner), but required hold violation threshold is 500ps. The above warning indicates that the hold violation threshold is 500ps. The endpoint of the poor path is t1daau_dp/dsmnbop 【 5 】 /opit_0/D , the cock is lclkp , the hold slack is -115ps under the fast corner , and the margin set by the user is 500ps ;

3) Solution: When reporting C:STA-3017 and W:Timing-4105 , the user can check the number of paths and the slack value indicated in the warning to determine whether the hold margin of the current project meets the expectations, which can be based on the actual project. Modify the desired hold margin value according to the situation: option "Place & Route" -> the value in "Fix Hold Violation Threshold For Clock Path Cross SRB(ps)", and then re-run place and route.

B. Layout module

【 Placement Decongestion Mode 】 Due to the complex user design and the strong

connection (Net) relationship between the logics, the layout algorithm may not be effectively diffused, and the layout density is high, which will adversely affect timing optimization and routing time. Set the area expansion coefficient according to the maximum proportion of the main resources (usually LUT , FF , APM , DRM) designed by the user. The setting value can be any integer from 【0,1,2,3,4,5,6,7,8,9】. In general, the larger the mode setting value, the larger the layout range and the faster the routing speed, but the timing will be worse. When the utilization rate of resources (LUT , FF , APM , DRM) exceeds 70% , and the larger the mode setting value is, the routing speed will become uncertain . 4 . The default value is 1 .

【 Placement Initial Method 】This option is used to select the initial position of the global layout. When this parameter is set to Center , it means that the starting position starts from the middle of the chip; when this parameter is set to Quad , it means that the starting position of the layout depends on the position constraints and IO layout results. The default is Quad .

【 Early Block Placement 】This option enables Macro Instance priority placement switch. When this option is checked, it means that Macro Instance is allowed to be placed first, which can speed up the wiring speed. When this option is not checked, Macro Instance is prohibited to be placed first . When this option is selected, the Auto Dispose Macro Object option can only be operated. This option is selected by default.

【 Auto Dispose Macro Object 】This option is the priority switch for PDS software to select macro modules adaptively. When this option is not checked, the user can select whether DRM , APM , DRAM , and Carry Chain are placed in priority through the Dispose DRM Prior , Dispose APM Prior , Dispose Distribute-RAM Prior and Dispose Carry Chain Prior options respectively . This option is selected by default.

【 Dispose DRM Prior 】 This option indicates that DRM will be placed first during layout . This option can be operated when Auto Dispose Macro Object is not checked . This option is selected by default.

【 Dispose APM Prior 】 This option indicates that APM should be placed first during layout . This option can be operated when Auto Dispose Macro Object is not checked . This option is selected by default.

【 Dispose Distribute-RAM Prior 】This option indicates that the Distribute-RAM will be placed first in the layout . This option can be operated when Auto Dispose Macro Object is not checked . This option is not selected by default.

【 Dispose Carry Chain Prior 】 This option indicates that the Carry Chain is placed first during layout . This option can be operated when Auto Dispose Macro Object is not checked . This option is not selected by default.

【 Design Cells Duplication 】: Layout algorithm timing optimization, using adaptive insertion and duplication logic cell algorithm to optimize layout timing. This option is selected by default.

【 RefinePlacement Mode 】 Layout algorithm timing optimization, the setting value can be selected in two modes【Swap, Bump】, the default is Swap mode. In Bump mode, only fine tuning is performed in units of instance , which is more suitable for small-scale devices. In Swap mode,

coarse adjustment is performed in units of Site , combined with fine adjustment in units of instance , which is more suitable for large-scale devices.

【 RefinePlacement Cluster 】Enable the packaging switch during the detailed layout process. When on, facilitates placement timing performance closure. This option is selected by default.

【 RefinePlacement Iteration 】This option is used to set the number of iterations for detailed layout convergence. When the detailed placement timing fails to close sufficiently, it is recommended to set this parameter to a larger value, and at the same time, the detailed placement closure time is longer. The default value is 20 .

【 Enable Recovery Analysis in GP 】 Enable recovery timing analysis in global placement. This option is not selected by default.

【 Enable Recovery Analysis in DP 】 Enable recovery timing analysis in detail placement. This option is not selected by default.

【 Enable Recovery Analysis in RP 】 Enable recovery timing analysis in replication placement. This option is not selected by default.

【 Placement Logic Optimization 】 Enables the placement logic optimization switch to optimize placement performance. When this option is checked, the program will perform logic optimization, and the current logic optimization only includes the LUT6D pack function. Only when this option is selected can the LUT6D Packing Strategy option be operated. This option is selected by default. (Only supports Logos2 series PG2L100H devices and Titan2 series PG2T390H devices)

【 LUT6D Packing Strategy 】 LUT6D pack function implementation strategy, use LUT6D to merge qualified LUTs in the layout stage to reduce LUT resources. The setting value is optional 【 0, 1, 2, 3 】 to indicate different pack strategies. The default value is 3 (only supports Logos2 series PG2L100H devices and Titan2 series PG2T390H devices)

【0】 : Turn off the LUT6D pack function;

【1】 : LUT6D pack (has a greater impact on performance)

【2】 : LUT6D pack (less impact on performance)

【3】 : LUT6D pack is performed , the number of LUT merging is relatively large (moderate impact on performance)

C. Wiring module

【 Enable Fast Router 】: Control whether to use global routing (compact does not support global routing) , this option is selected by default.

【 Fast Router Mode 】: Control the mode of global routing, divided into automatic selection mode (Auto), non-disconnect mode (Mode1), and disconnect mode (Mode2). The default is Auto . (This option is only available for Titan series devices)

【 Enable multi-thread routing 】: Control the switch of multi-thread routing mode. This option is selected by default (only Titan2 series devices have this option)

【 Thread size 】: Control the number of threads for multi-threaded wiring. This option can be operated when Enable multi-thread routing is checked. The default value is 8. (This option is only available for Titan2 series devices)

【 Reduce CE/RS signal 】: Used to control whether to use Control Chain. This option is selected by default.

【 CE/RS signal series limit 】 The maximum length of CE/RS control signal chain. The default value is 500 .

【 Enable Global IOCLKGATE 】: Controls whether the clock wiring automatically uses IOCLKGATE, this option is not selected by default. (This option is only available for Titan series devices)

【 Slack Prior In Global router 】 Controls whether to use the Slack Prior In Global router. It can only be used when Enable Fast Router is checked, and this option is selected by default. (compact does not support global routing)

【 Slack Weight 】 Controls the weight of timing factors in the routing process. The default value is 90.

【 Pin Cost Increasing Speed 】 Control the speed at which the congested port increases the cost value. The default value is 300.

【 Max iterations in congest mode 】This option is used to set the maximum number of routing iterations in control congestion routing mode. The default value is 200.

【 Dump Router Congestion Plot 】 This option is used to set whether to print the congestion node file. When checked, when running the routing process, the CongestionPlot and CongestionNetInfo folders will be created in the place_route directory to record the congested node files and the net information of routing conflicts generated during each iteration of the detailed routing process, respectively. This option is not selected by default.

Right-click anywhere in the Report Summary -> Flow Summary of PDS and select " Open Congestion Plot " to open the congestion map, automatically load the congestion node file in the CongestionPlot , and visualize the congestion situation of each iteration of the detailed routing.

Congestion map page function introduction:

The left side of the congestion graph shows the congested node files generated in each round;

SRB is displayed according to the selected congestion node file ;

The max value is : * " in the lower right corner records the maximum congestion value on the SRB of this iteration ;

SRB Conflict(max color mapping) " in the lower left corner . The congestion value on each SRB in the congestion map is adaptively adjusted according to the set maximum value. The scalar displays different colors . the greater the congestion;

Support SRB search function, search for the specified SRB in the search box in the upper right corner , it will mark the searched SRB as the center on the congestion map , and expand 4 tiles up , down, left and right ;

Supports CongestionPlot file replacement, and the congestion node files generated by other projects can be loaded at the top of the page.

【 Enable Recovery Analysis in Routing 】 Enable recovery timing analysis in routing. This option is not selected by default.

【 Check Clock Net Routing Path 】 Check whether the clock signal uses a non-clock tree path for routing. If it is enabled, when the clock signal uses a non-clock tree path, the path will be alarmed, and the Critical Warning information will be printed in the Console : *C: Route-2036* . This option is selected by default.

D. Run the module multiple times

【 Global Placement Random Seed 】 The layout algorithm of PDS belongs to the global optimization algorithm, which depends on the initial value. Different initial values will obtain different algorithm optimization effects. The main function of this parameter is to provide random positions for the placement algorithm, so that the user can obtain the placement and routing results with the best performance. The default value is 0.

【 Placement Iterations 】 The number of times to perform multiple sub-placement and routing, the minimum is 1. The default value is 1 .

【 Placement Random Seed Step 】 The seed step size for performing multiple sub-placement and routing. The default value is 1 .

【 Placement Save Best Run 】 The number of saved optimal results for performing multiple sub-placement and routing operations. The default value is 1 .

【 Maximum Number Of Mutil-seed Running In Parallel 】 The maximum number of parallel execution of multiple seeds. The default value is 1 .

【 Filter Strategies 】 Set the filter conditions for filtering the best seeds, the highest priority. The default value is empty.

【 Sort Strategy 】 Set the sorting rules for filtering the best seeds, the next highest priority. The default is setup .

【 Timeout 】 Set the maximum running time of each seed, the timeout will automatically terminate the task; it will take effect when it is greater than 0 , and the unit is minutes. The default value is 720 .

【 Generate Bitstream In Multi-seed Mode 】 Set whether to generate bitstream after PnR is completed. This option is not selected by default.

After completing the setting, perform the 【 Place & Route 】 operation.

In the process of running the placement and routing, multiple seeds are reserved for the seed

screening rules: the optimal seed results are firstly screened by the rules set by the user, and Filter Strategies is the first priority. The user can set the corresponding slack value range of setup , hold , recovery , and removal . Sub-priority Sort Stratrgy , the user can specify the sorting priority strategy, the default sorting priority: setup>hold>recovery>removal , if the user specifies the sorting as hold , except the specified sorting item hold is the first priority, the rest are based on the default priority Filter the seeds (that is, when the corresponding slack value of hold is the same, compare the corresponding slack values of setup, recovery, and removal in turn) , sort the seed results , and finally retain the filtered seed results according to the 【 Placement Save Best Run 】 set by the user.

All seed results are aggregated in multiseed_result.csv , which satisfy the filter conditions set by the user, marked with UserFilter=1 in the table, and 0 otherwise .

Note: The four options that can be set in FilterStrategies and Sort Strategy are setup/hold/recovery/removal to compare the corner values of slow and fast to take the smaller value.

Eight results of multiple sub- setup/hold/recovery/removal in slow and fast corners are retained in multiseed_result.csv .

In addition, during the running process, you can also click Show Multi-Run State to view the running status, and you can manually terminate the running of the corresponding seeds, as shown in the following figure:

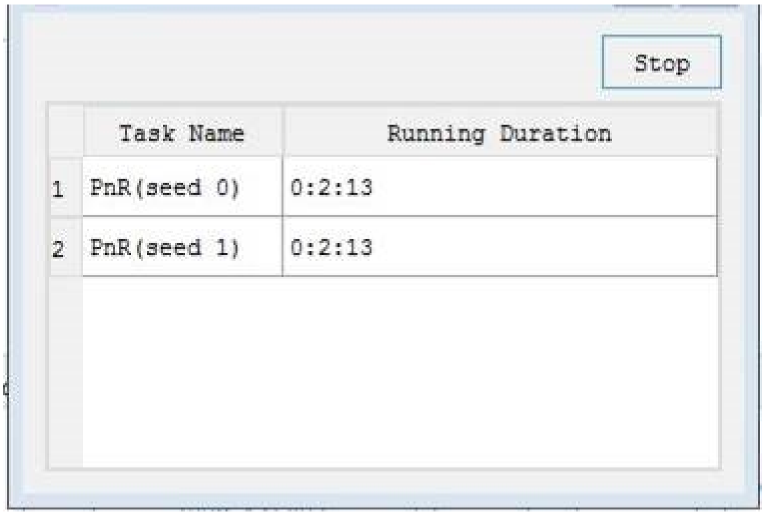


Figure 3-27 Place & Route Multi-Run State interface

After running layout and routing, the interface is as follows:

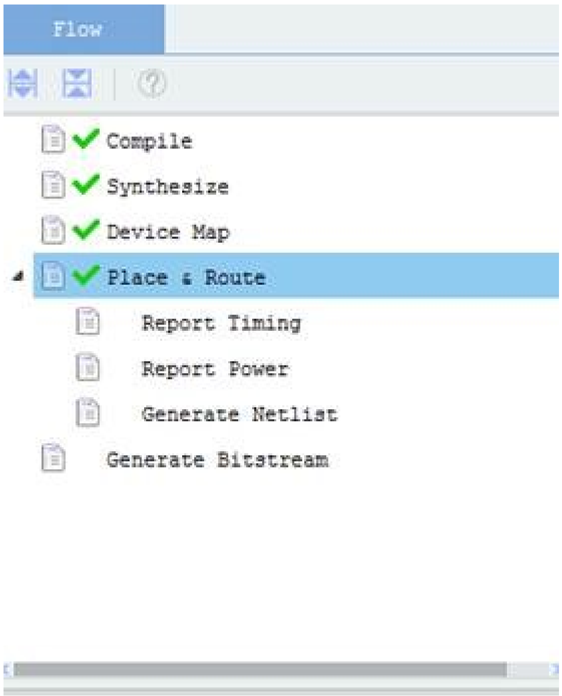


Figure 3-28 Place & Route software interface after running

The user specifies any seed to run the process after pnr by right-clicking the PNR and selecting a Seed To Apply .

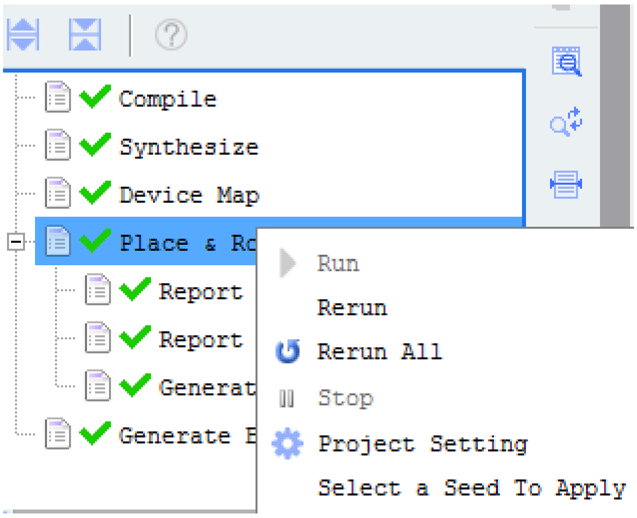


Figure 3-29 Place & Route right-click interface

The user selects a Seed To Apply by right-clicking on the PNR to specify any seed to run the process after pnr .

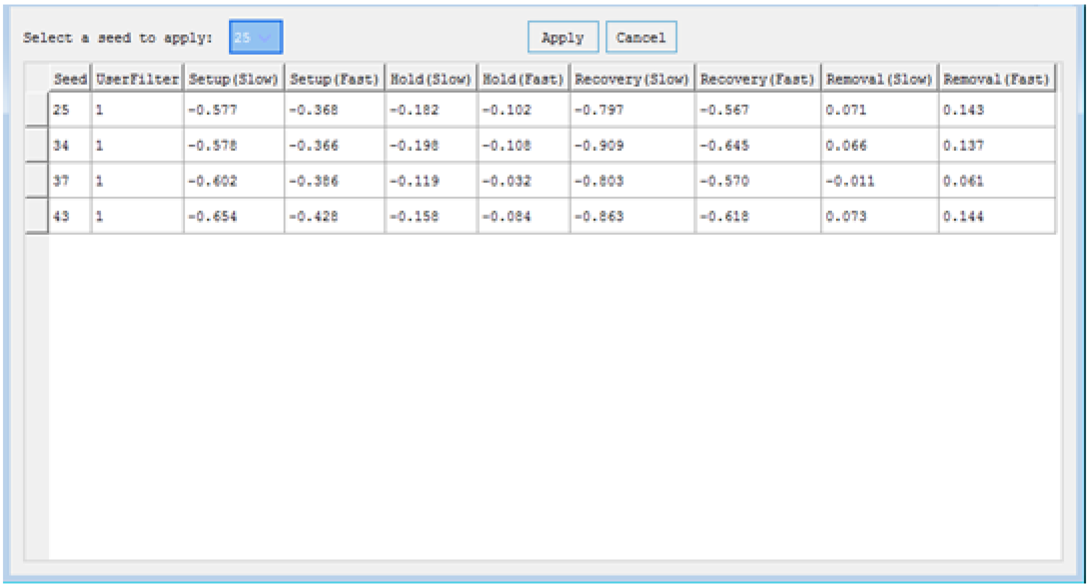


Figure 3-30 Place & Route Select a Seed To Apply interface

5) Wiring automatic iteration module

This module supports automatically extracting nets that do not meet the setup slack according to the set value , generates the route_constraint_ite.rcf file in each iteration, sets the priority routing constraint instructions for the net , and accumulates the constraint instructions of each iteration to all_route_constraint_ite.rcf in the Place_Route directory In the next round of placement and routing iterations , the priority routing instructions in all_route_constraint_ite.rcf will be reloaded, and the iteration process will not exit until the set maximum number of iterations is reached or the setup slack threshold condition corresponding to net is met.

best iteration result is kept in the all_route_constraint_ite.rcf file.

rcf file is not added to the customer project , the " all_route_constraint_ite.rcf " file accumulated in the PR directory will be used after the automatic routing iteration. If you want to use the result after the routing iteration, you can open the RCE to load the file and run the PR process again. ; If there is an original user_rcf file, the routing uses the set of constraint commands in the two files user_rcf+ all_route_constraint_ite.rcf . If you want to re-run the whole process of PR , you need to manually summarize the results of the two rcf files to user_rcf .

[Enable Route Constraint Iterate] The routing iteration switch is used to decide whether to turn on or off the automatic iteration. By default, the routing iteration is not checked if it is not checked. After checking, the routing automatic iteration will be performed according to the relevant configuration. This option is not selected by default.

[Route Constraint Iterate Times] Execute the maximum number of automatic routing iterations. When the number of iterations reaches the maximum, the iteration will be automatically terminated. The default value is 10 times.

[Route Constraint Slack Value(ns)] Specifies the setup slack threshold corresponding to the net that generates the rcf . If not set, the default value is 0 .

[Route Constraint Max Timing Path] specifies the maximum number of timing paths reported by timing in each iteration , If not set, the default value is 3 .

number of iterations and the setup slack threshold corresponding to net are also the conditions for the exit of the wiring iteration. If any one of the conditions is met, the automatic wiring iteration process will be exited.

Note: Routing automatic iteration currently does not support joint use with the multi-sub-layout function in Multi-Run .

3.4.2 Place & Route Report

PNR is over (including Place Only), Place & Route in Report Summary can view the layout and routing report, as shown in the following figure:

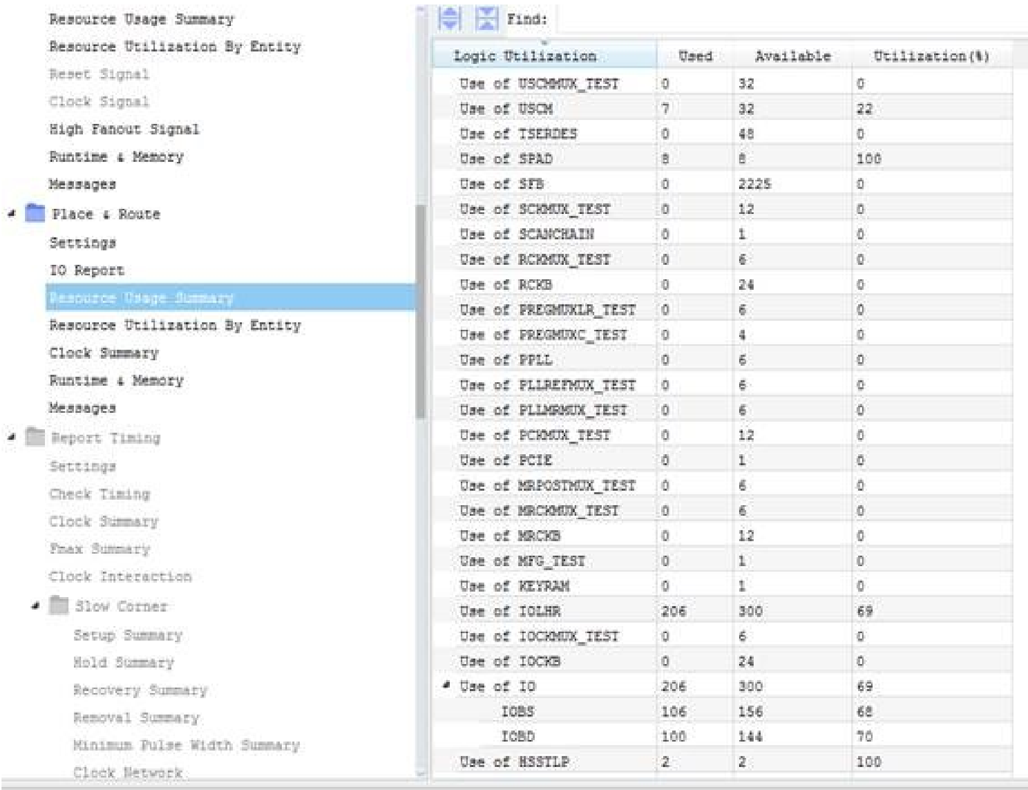


Figure 3-31 Place & Route Resource Usage Summary interface

1) Clock Summary

Global Clock , Region Clock , Horizontal Clock , and PLL Clock reports of the layout .

Global Clock (USCM , USSMBUF) report content: global clock instance (GClkInst), global clock layout location (SiteOfGClkInst), global clock fanout line (GClk_Fanout_Net), global clock fanout (Fanout), global clock driver source (DriverInst) , The layout location of the global clock driver source (SiteOfDriverInst).

Region Clock (RCKB) report content: regional clock instance (RClkInst), layout location of regional clock (SiteOfRClkInst), regional clock fanout line (RClk_Fanout_Net), regional clock fanout (Fanout), driving source of regional clock (DriverInst) , regional clock Layout location of the clock driver source (SiteOfDriverInst).

Horizontal Clock (HCKB) report content: horizontal clock instance (HClkInst), horizontal clock layout location (SiteOfHClkInst), horizontal clock fanout line (HClk_Fanout_Net), horizontal clock fanout (Fanout), horizontal clock driving source (DriverInst), horizontal clock Layout location of the clock driver source (SiteOfDriverInst).

PLL Clock (PLL , GPLL , PPLL) report content: PLL clock instance (PllInst), PLL clock layout position (SiteOfPllInst), PLL clock port (Pin): including input, output, PLL clock port connection line (NetOfPin), PLL Clock fanout (Fanout) , PLL clock driving source or load (Driver(Load)Inst) , PLL clock driving source or load layout location (SiteOfDriver(Load)Inst) .

PLL Clock report content are: for the clock input pin , it has no Fanout value, and the display is "-" , for the clock output pin , if the pin is floating, the Fanout value displays "0" ; if the clock pin is floating, then the value displayed by NetOfPin , Driver(Load)Inst , SiteOfDriver(Load)Inst is "nullptr" ; for the clock output pin , if the value of Fanout is greater than 1 , the value displayed by Driver(Load)Inst and SiteOfDriver (Load)Inst is "..." .

2) clock_utilization.txt

The detailed statistical report of clock planning information is uniformly recorded in the directory clock_utilization.txt of place_route .

clock_utilization.txt is described as follows:

Clock Regions-Block Scope table: This type of chip is divided into the number of blocks and the Floorplan coordinate range of each block, which is consistent with the Floorplan used by the resources in the UCE or PCE tool , starting from the lower left corner of the chip.

Clock Regions-Clock Primitives table: Statistics of available clock resources and logic resources information in each region of the chip (only CLM , DRM , APM are counted), such as logos2 series statistics are CLK PAD , PLL PAD , RCKB , IOCKB , HCKB , MRCKB , CLMA , CLMS , DRM , APM and other resource information quantity.

Among them, the BRGCLKGATE and some IOCLKGATEs of PGT180H cross regions and are not counted; IOCLKGATEs are classified according to the region where the load (excluding Clock Buffer) they drive is located. IOCLKDIV is classified according to the corresponding IOCLKGATE.

User constraint information is clock information before layout. Statistics are collected and counted according to the global clock, regional clock, and IO clock network classification. When making statistics, the clock system circuit is decomposed into clock sub-circuits according to Source, Buffer , and Load . Clock Source and Clock Buffer do not support Region constraints, but physical constraints.

format of the display interface of Global/Regional/IO Constraint is the same, the following uses Global Constraint as an example to illustrate.

Global Clock Buffer Constraint Details table: mainly collects the constraint information of Clock Buffer-loads , the meaning of each column:

1. Source Name : the Instance name of the clock source of the clock subcircuit ;
2. Source Pin : the name of the Pin that outputs the clock signal from the clock source of the clock subcircuit ;
3. Source - Buffer Net : the name of the Net connected between the clock source Source and the clock core component Buffer in the clock sub-circuit ;
4. Buffer Input Pin : The name of the Input Pin of the clock core component Buffer in the clock sub-circuit, which is the Pin that receives the clock signal ;
5. Buffer Name : the name of the clock core component Buffer Instance in the clock sub-circuit ;

6. Buffer Output Pin : The name of the Output Pin of the clock core component Buffer in the clock sub-circuit, which is the pin that outputs the clock signal ;

7. Buffer-Load Net : the name of the Net that connects the Output Pin of the clock core component Buffer and Load in the clock sub-circuit ;

8. Clock Region Of Buffer Site : If the user has set a constraint on the Buffer , it will display the area number of the constraint position, and if it is not constrained, it will display " --- ";

9. Buffer Site : If the user sets constraints on the Buffer , the specific constraint location will be displayed, that is, the name and coordinates of the Grid Device where the resource is located;

10. IO Load Clock Region : Load is the regional limitation of IO type , which is controlled by the clock core component Buffer of the driver and user constraints;

11. Non - IO Load Clock Region : Load is not restricted by the IO type area, and is controlled by the clock core component Buffer of the driver and user constraints;

12. Clock Loads : Load is to use the information transmitted from Buffer as a clock signal and count its quantity;

13. Non-Clock Loads : Load is to use the information sent by the Buffer as an ordinary data signal, and count its number.

Global Clock Source Constraint Details table: mainly collects the constraint information of Clock Source , the meaning of each column:

1. Source Name : the Instance name of the clock source of the clock subcircuit ;

2. Source Pin : the name of the Pin that outputs the clock signal from the clock source of the clock subcircuit ;

3. Source-Load Net : The name of the Net connected between the Pin of the clock subcircuit clock source output clock signal and its Load ;

4. Clock Region Of Source Site : If the user has set a constraint on the Source , it will display the region number of the constraint location, and if it is not restricted, it will display " --- ";

5. Source Site : If the user sets a constraint on the Source , it will display the specific constraint location, that is, the name and coordinates of the Grid Device where the resource is located;

6. Clock Buffer Loads : Count the number of Clock Buffers connected behind the Source (the PGT180H device will copy 4 copies of the USCM , but the Global Clock Buffer Constraint Details will only display the original Clock Buffer , and the actual layout will retain the corresponding USCM according to the location of the load , and delete the excess Lose);

7. Non - Clock Buffer Loads : Count the number of non- Clock Buffer Instances connected behind the Source .

The clock layout information is the layout information in the clock planning stage, not the final layout information. The statistical method is consistent with the user constraint information. Take Global Clock as an example below.

Device Cell Placement Summary for Global Clock Buffer table: mainly collects the planning information of the clock automatic layout of the Clock Buffer, and the meaning of each column can be explained by referring to the Global Clock Buffer Constraint Details table.

Among them, IO Load Clock Region and Non-IO Load Clock Region are based on the driving range determined by the layout position of Buffer and its driving load .

Device Cell Placement Summary for Global Clock Source table: mainly collects the planning information of Clock Source 's clock automatic layout, and the meaning of each column can be explained by referring to the Global Clock Source Constraint Details table.

If the clock planning fails, detailed planning failure information will be printed, including failure reasons and solutions to failure problems.

Placement Failed Information About The Constraint Details Of Buffer table: Buffer information of clock core components that fail to be planned . For the meaning of each column, refer to the Device Cell Placement Summary for Global Clock Buffer table.

Placement Failed Information About The Load Of Source Instance table: Instance information of the clock source that failed to plan , meaning of each column:

1. Driver Pin : the name of the Pin where the clock source of the clock subcircuit outputs the clock signal ;

2. Driver-Load Net : The name of the Net connected between the Pin of the clock subcircuit clock source output clock signal and its Load ;

3. Load Instance : the name of the clock core component Buffer Instance in the clock sub-circuit ;

4. Load Unit : the realization of the clock core component Buffer Instance in the clock sub-circuit ;

5. Load Clock Region : If the user has set a constraint on the Buffer , it will display the region number of the constraint position, and if it is not constrained, it will display " --- ";

Placement Failed Information About The Load Of Buffer Instance : Buffer Drive Load information of the clock core component that failed to plan , the meaning of each column:

1. Driver Pin : the name of the Output Pin of the clock core component Buffer in the clock sub-circuit, which is the pin that outputs the clock signal ;

2. Driver-Load Net : the name of the Net that connects the Output Pin of the clock core component Buffer and the Load in the clock sub-circuit ;

3. Load Instance : the load driven by the clock core component Buffer Instance in the clock sub-circuit ;

4. Load Unit : Buffer Instance , the core component of the clock in the clock sub-circuit, drives the load ;

5. Load Clock Region : The regional limitation of Load is controlled by the core clock component Buffer of the driver and user constraints .

3.5 Report Timing

3.5.1 Report Timing Settings

Report_Timing_settings are introduced as follows: Report Timing option settings, as shown in the figure below:

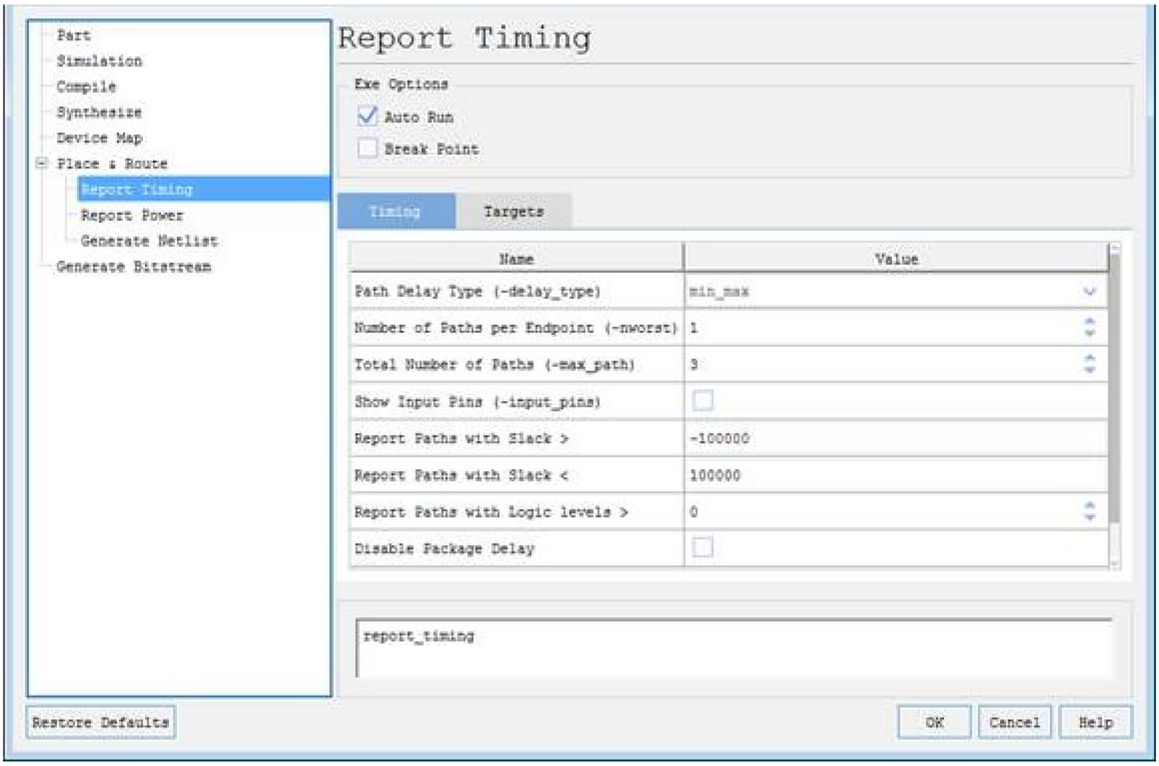


Figure 3-32 Report Timing option settings

Report configuration options:

Timing Analysis

【 Path Delay Type (-delay_type) 】 Set the type of timing analysis, the options are "max", "min", "min_max" . Selecting max will only perform setup analysis on the timing path, selecting min will only perform hold analysis on the timing path, and selecting min_max will perform setup and hold analysis on the timing path. The default is min_max .

【 Number of Paths per Endpoint (-nworst) 】 Set the maximum number of paths reported by the endpoint of each timing path. The default value is 1 .

【 Total Number of Paths (-max_path) 】 Sets the maximum number of paths for timing reporting. The timing analysis tool sorts the timing paths according to slack , the maximum number of paths will not exceed the number set by this item, and the default value is 3 .

【 Show Input Pins (-input_pins) 】 Show input Pins . If this option is selected, the input port information will be displayed in the timing path . If this option is not selected, the input port information will not be displayed in the timing path , and this option is not selected by default.

【 Report Paths with Slack > 】 Set the minimum range of slack for the report. Timing paths whose slack is smaller than the setting of this item will not be displayed. The default value is -100000 .

【 Report Paths with Slack < 】 Set the maximum range of slack reported. Timing paths whose slack is greater than the setting of this item will not be displayed. The default value is 100000 .

【 Report Paths with Logic Levels > 】 Set the minimum range of Logic Levels reported. Timing paths whose Logic Levels are less than or equal to this value in setup/recovery timing analysis will not be displayed. This setting does not affect hold/removal analysis timing paths. The default value is -1 .

【 Disable Package Delay 】 Set timing report whether to calculate package (package pin) delay. If checked, package delays will not be included in the timing report path, and the option is unchecked by default.

[Report IO Datasheet] Set whether the timing report reports the timing characteristics of IO , including Input Ports Setup/Hold , Output Ports Clock-to-out , Combinational Delays , Setup/Hold times for input bus , Max/Min delays for output bus . This option is not selected by default.

[Report Max Skew] Set whether the timing report reports the timing characteristics of the user-constrained set_max_skew command. If this option is not selected , the final timing report will not report relevant content even if there is a set_max_skew command constraint. This option is not selected by default.

* Note: When executing Place & Route and Placement Iterations is greater than 1 (i.e. running in multi-seed mode), the system will execute Report Timing in the background and select the optimal result according to the slack value of the generated report ; if Path Delay Type (-delay_type) If the option is set to min , then slack -related information will not be output , and the result of Place & Route operation is undefined.

[Skip DB version check] If the old version of the project has run to pnr or report timing , the new version of the software will open the old version of the project. After checking this option, you can only run report timing to generate a timing report without rerun all . This option is not selected by default (Devices currently supporting this option only support PG2T390H , PGL25G , PG2L100H , PGT180H)

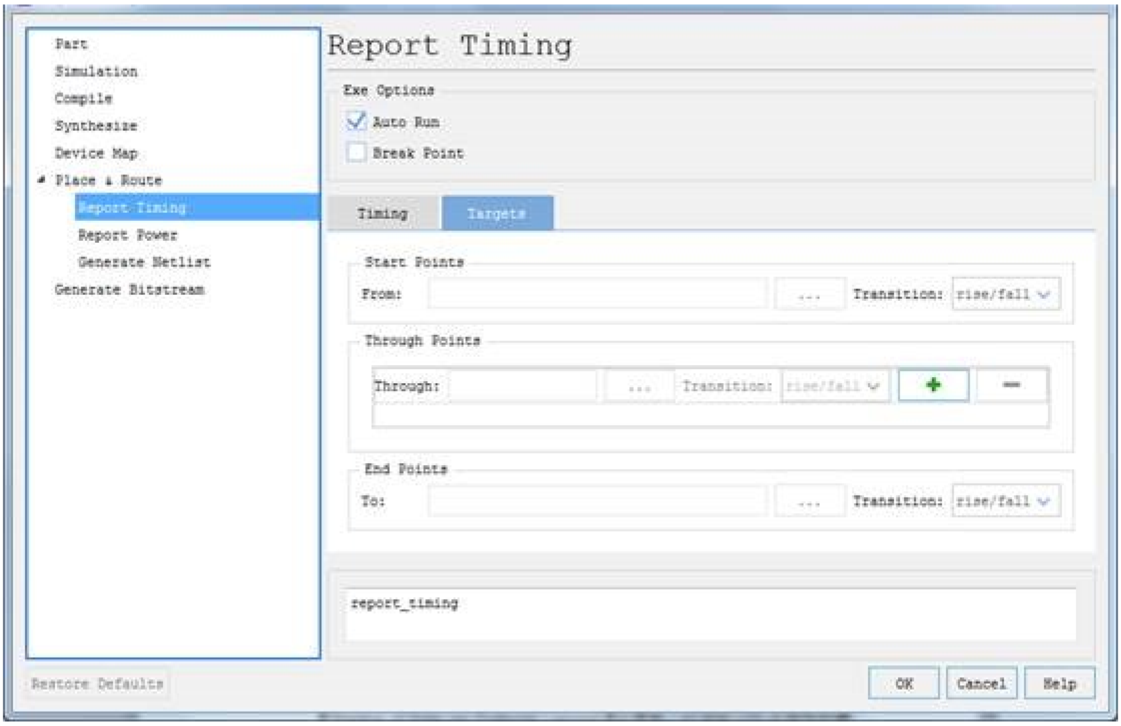


Figure 3-33 Report Timing option settings

【 From 】 【 Through 】 【 To 】 You can specify the from/through/to nodes of the timing path in the timing report . The default values are all empty.

3.5.2 Report Timing report

The timing report has the following items: Settings , Check Timing , Clock Summary, Fmax Summary , Clock Interaction , Timing Path Report and IO Datasheet . The Timing Path Report includes the Timing Path reports of the two extreme cases of Slow Corner and Fast Corner . The Timing Path reports of these two Corners include Setup Summary , Hold Summary , Recovery Summary , Removal Summary , Minimum Pulse Width Summary and Worst Case Timing Path , Worst Case Timing Path has been distinguished from Setup , Hold , Recovery , Removal , and Minimum Pulse Width . The directory tree corresponding to Timing Report is shown in the figure below.

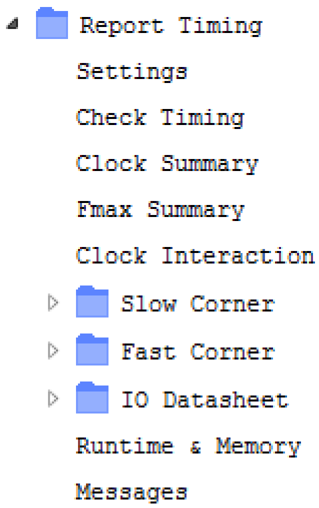


Figure 3-34 Directory tree corresponding to Timing Report

If the timing requirements are not met, the nodes on the directory tree will be displayed in red for quick location and viewing.

1. Settings

Displays the settings of the current timing analysis, the specific items are as shown in the figure below:

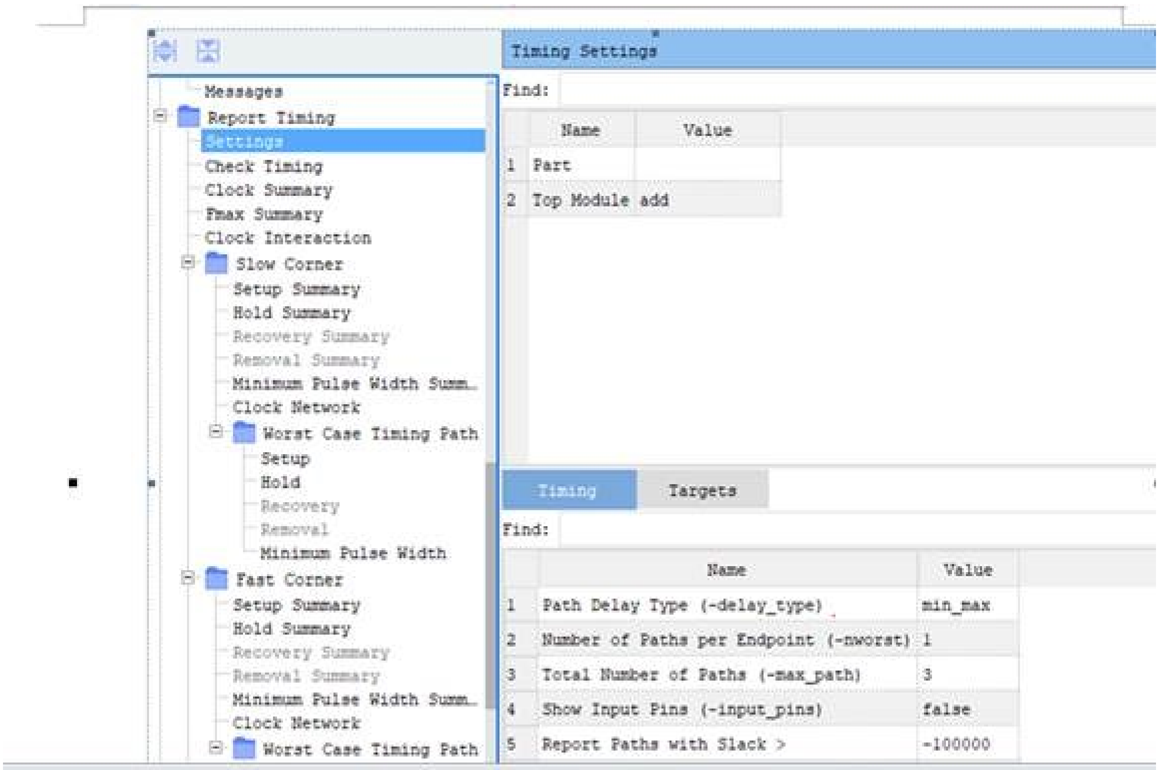


Figure 3-35 Report Timing Settings

2. Check Timing

Check Timing is to check the timing constraints in the current design before the timing analysis is performed, as shown in the figure below:

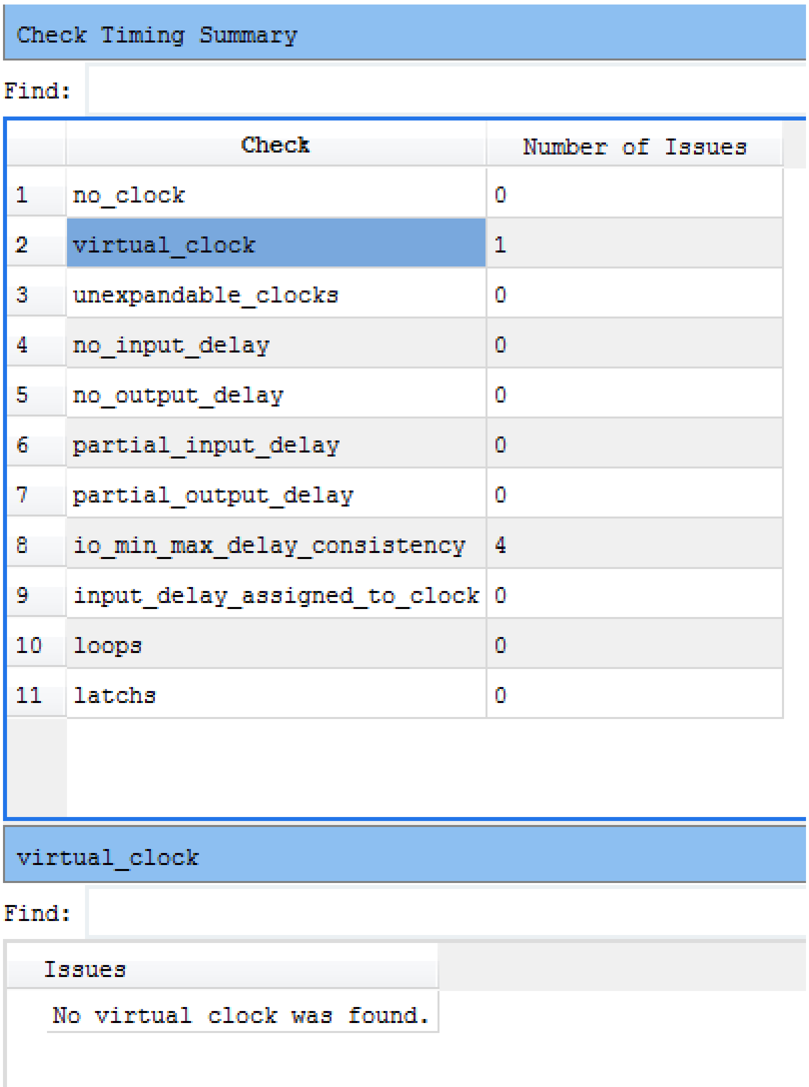


Figure 3-36 Check Timing Report Summary

The main check items and introduction of Check timing are as follows:

1) no_clock

This check is mainly used to check whether the clock port of the sequential device has a clock driver (clock propagate). If the clock port of the sequential device has no clock data, the timing analysis cannot perform timing analysis such as setup and hold for the sequential device ;

2) virtual_clock

This check is used to check whether a virtual clock is created in the design , or a virtual clock is set but not used.

3) unexpandable_clocks

This option checks whether a common period can be found within 1000 cycles between asynchronous clocks .

4) no_input_delay

This item checks that the input port does not have set_input_delay set .

5) no_output_delay

The check output port does not have set_output_delay set .

6) partial_input_delay , partial_output_delay

This item checks the setting of the delay constraint of the input port, and only set_input_delay –max or set_input_delay –min exists for an input port . Setting a delay constraint on the port part will prevent the timing analysis tool from performing a comprehensive timing analysis on the path . If the constraint delay set on a port does not specify -min or -max , the timing analysis tool will assume that the port has the same min and max delay .

7) partial_output_delay

This item checks the settings of the output port delay constraint. Only set_output_delay –max or set_output_delay –min exists for an output port . Setting a delay constraint on the port part will prevent the timing analysis tool from performing a comprehensive timing analysis on the path . If the constraint delay set on a port does not specify -min or -max , the timing analysis tool will assume that the port has the same min and max delay .

8) io_min_max_delay_consistency

This item checks the consistency of the constraint settings of the IO delay , and checks the settings of set_input_delay and set_output_delay . If the min delay of the IO delay is greater than or equal to the max delay , a warning is reported . For the IO delay constraint that does not specify min and max , the software defaults that min and max delay are equal, and it also needs to be reported.

9) input_delay_assigned_to_clock

This option checks whether the input delay is set to the clock port, in which case the input delay will be ignored.

10) Loops

Check whether there is a combination loop in the design , the combination loop may not be analyzed correctly.

11) latches

Check if there is a latch in the design .

3. Clock Summary

Display basic information about the clock.

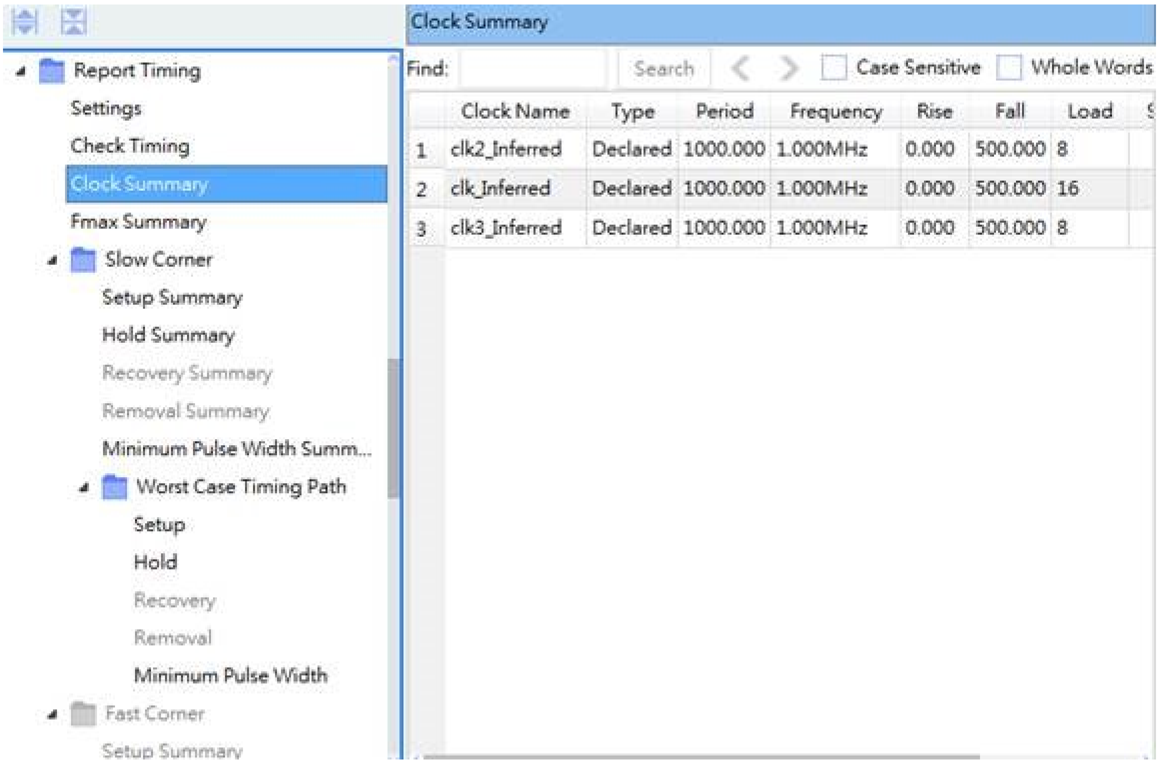


Figure 3-37 Clock Summary

4. Fmax Summary

Displays the maximum operating frequency of the clock. The Fmax of the clock is calculated based on the timing path with the smallest slack in the same clock domain. Timing paths across clock domains will not affect the Fmax result . Since the calculation of Fmax does not consider the timing path across clock domains , this result is only used as a reference for clock performance and cannot be used as a basis for judging timing convergence.

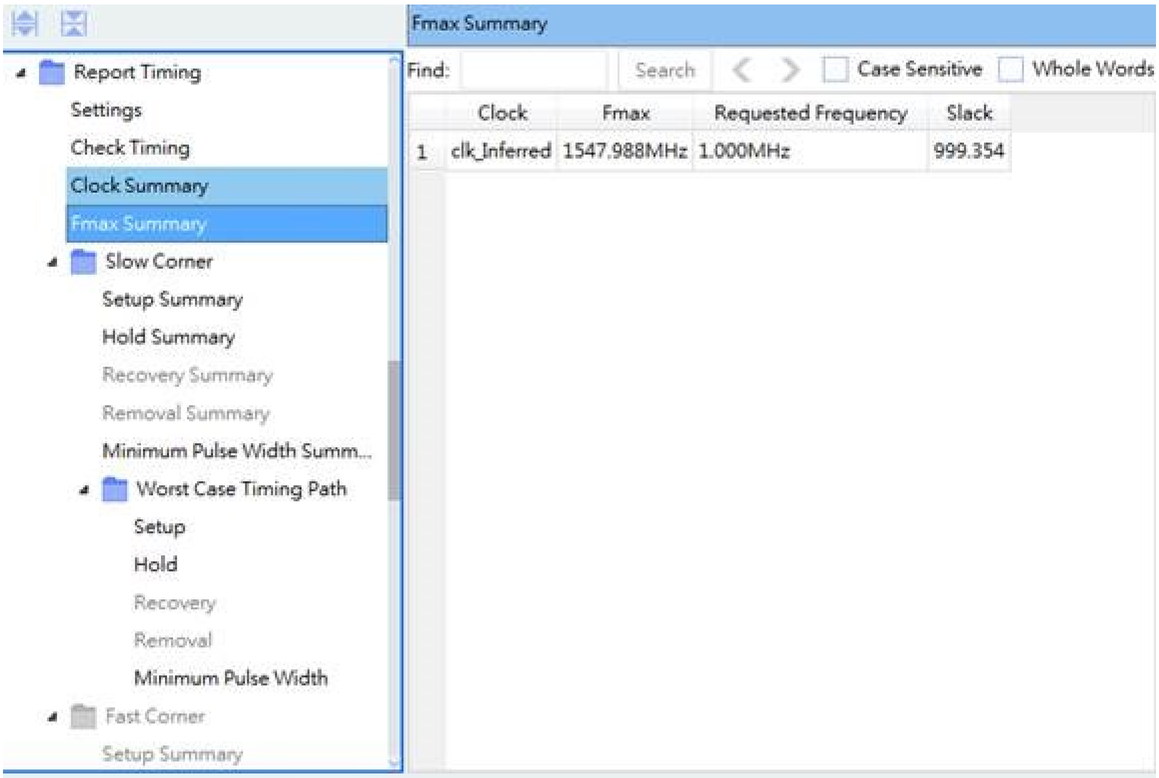
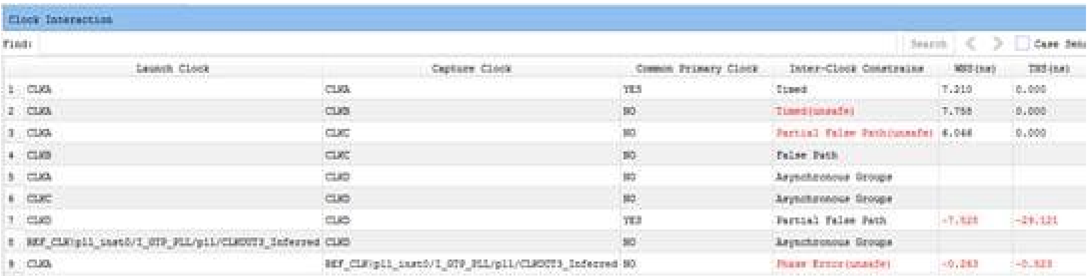


Figure 3-38 Fmax Summary

If the maximum operating frequency of the clock does not meet the user's constraints, that is, Fmax < Requested Frequency , the line where the clock is located will be marked in red.

5. Clock Interaction Report

Clock Interaction Report is used to report the relationship between clocks and timing constraints in the design , as shown in the following figure:



	Launch Clock	Capture Clock	Common Primary Clock	Inter-Clock Constraint	WNS(ns)	TNS(ns)
1	CLKA	CLKA	YES	Timed	7.310	0.000
2	CLKA	CLKB	NO	Timed(unsafe)	7.758	0.000
3	CLKA	CLKC	NO	Partial False Path(unsafe)	6.048	0.000
4	CLKB	CLKC	NO	False Path		
5	CLKA	CLKD	NO	Asynchronous Groups		
6	CLKC	CLKD	NO	Asynchronous Groups		
7	CLKD	CLKD	YES	Partial False Path	-7.325	-29.121
8	REF_CLK|pll_inst0/I_GTP_PLL/pll/CLKOUT3_Inferred	CLKD	NO	Asynchronous Groups		
9	CLKA	REF_CLK|pll_inst0/I_GTP_PLL/pll/CLKOUT3_Inferred	NO	Phase Error(unsafe)	-0.263	-0.323

Figure 3-39 Clock Interaction Report

The main contents of the report are as follows:

Launch Clock : Indicates the launch clock.

Capture Clock : Indicates the receiving clock.

Common Primary Clock : Indicates whether the main clocks of the transmitting clock and the receiving clock are consistent.

Inter-Clock Constrains : Indicates the relationship between the transmitting clock and the receiving clock, which has the following relationships:

o Timed : Indicates that the transmit and receive clocks are synchronous clocks, and the path between the two is safely constrained.

o Timed(unsafe) : Indicates that the transmit and receive clocks are asynchronous clocks, and the path between the two is not constrained.

o False Path : Indicates that all paths between the transmit and receive clocks are defined as false paths by the command set_false_path .

o Partial False Path : Indicates that the transmit and receive clocks are synchronous clocks, and a part of the path between them is defined as a false path by the user using the command set_false_path .

o Partial False Path(unsafe) : Indicates that the transmitting and receiving clocks are asynchronous clocks, and a part of the path between them is defined as a false path by the user using the command set_false_path .

o Asynchronous Groups : Indicates that all paths between the transmit and receive clocks are defined as false paths by the command set_clock_groups .

o Phase Error(unsafe) : Indicates that at least one of the transmit and receive clocks is a generated clock , and the phase relationship between the generated clock and another clock cannot be determined, indicating that the timing path between these two clocks is unsafe .

o Max Delay Datapath Only : Indicates that all paths between the transmit and receive clocks are constrained by set_max_delay –datapath_only .

WNS : Indicates the worst slack of all setup and recovery paths between transmit and receive clocks .

TNS : Indicates the sum of all slack values less than 0 for all setup and recovery paths between the transmit and receive clocks .

Failing End Point(TNS) : Indicates the number of end points with slack less than 0 in all setup and recovery paths between the transmit and receive clocks .

Total End Point(TNS) : Indicates the number of end points in all setup and recovery paths between the transmit and receive clocks .

WHS : Indicates the worst slack of all hold and removal paths between transmit and receive clocks .

THS : Indicates the sum of all slack values less than 0 for all hold and removal paths between the transmit and receive clocks .

Failing End Point(THS) : Indicates the number of end points with slack less than 0 in all hold and removal paths between the transmit and receive clocks .

Total End Point(THS) : Indicates the number of end points in all hold and removal paths between the transmit and receive clocks .

6. Clock Network Report

Clock Network Report is used to report the clock path and path delay in the user design , located under the Slow Corner and Fast Corner directories, as shown in the following figure:

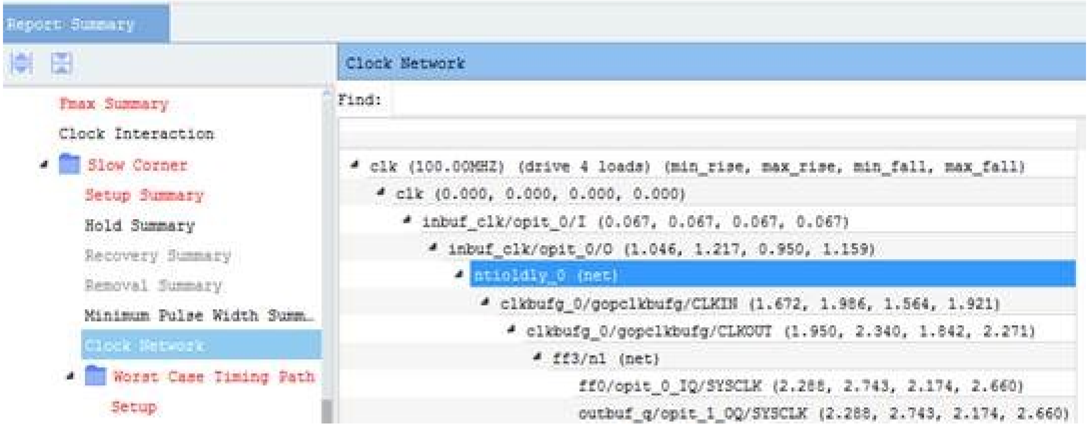


Figure 3 -40 Clock Network Report

7. Timing Path Report

o Setup Summary

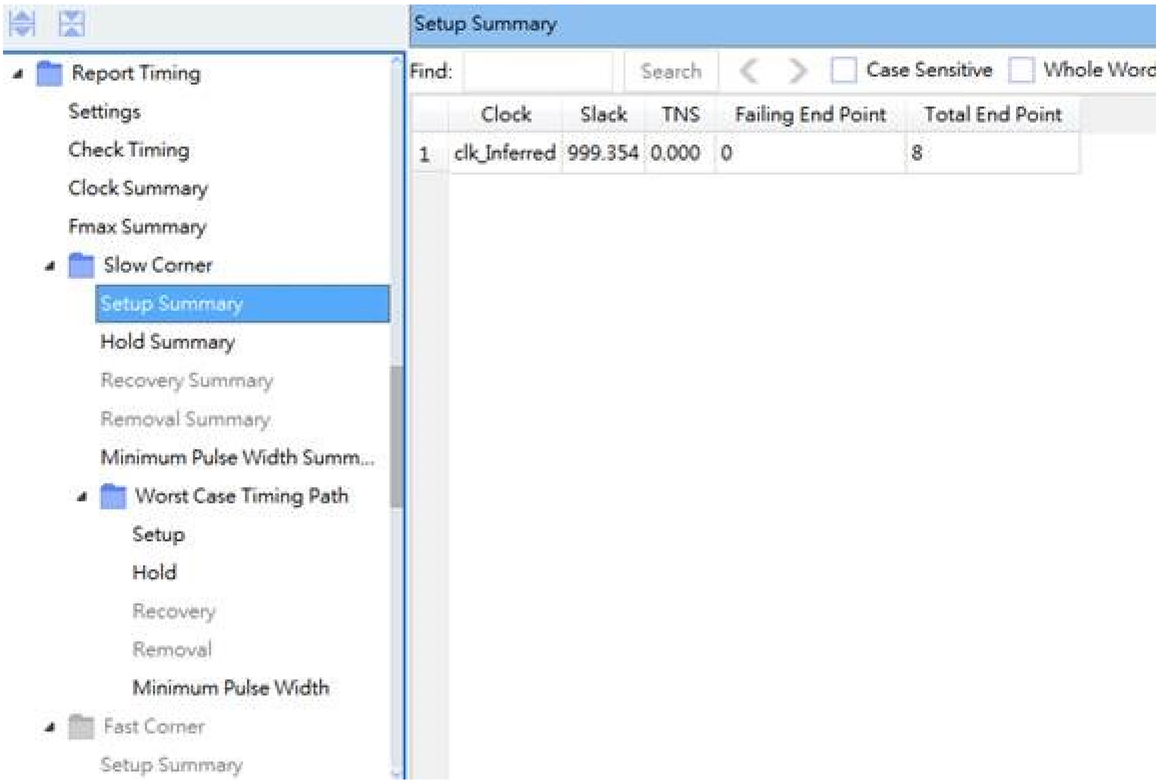


Figure 3-41 Setup Summary

The figure above , Launch Clock is the name of the defined launch clock, and Capture Clock is the name of the defined receive clock; Slack refers to the minimum value of slack in the setup path group where the two clocks are located; Total Negative Slack (TNS) indicates the The sum of all slacks less than 0 in the setup path group where a clock is located ; Failing End Point indicates how many End Points driven by these two clocks have timing failure; Total End Point indicates how many End Points driven by these two clocks .

o Hold Summary

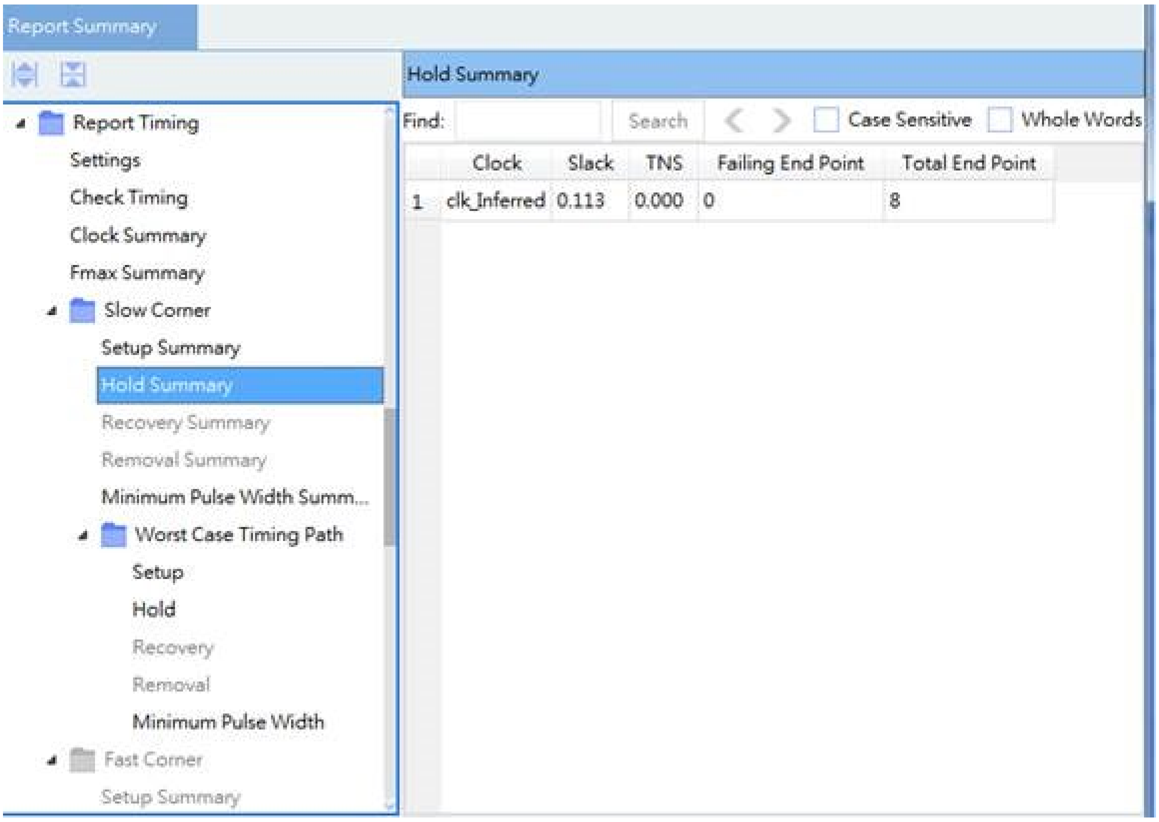


Figure 3-42 Hold Summary

o Recovery summary

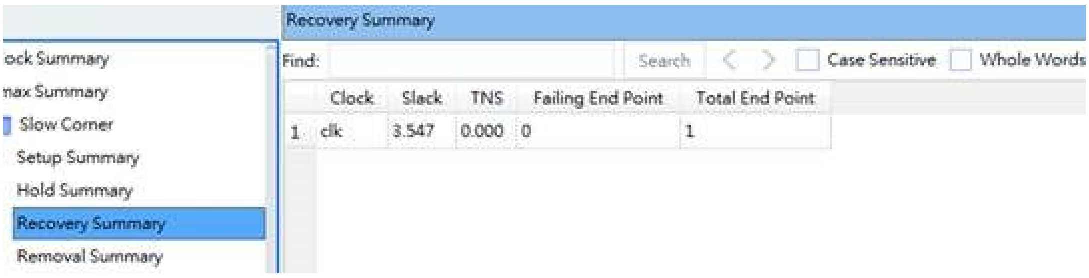


Figure 3-43 Recovery Summary

o Removal summary

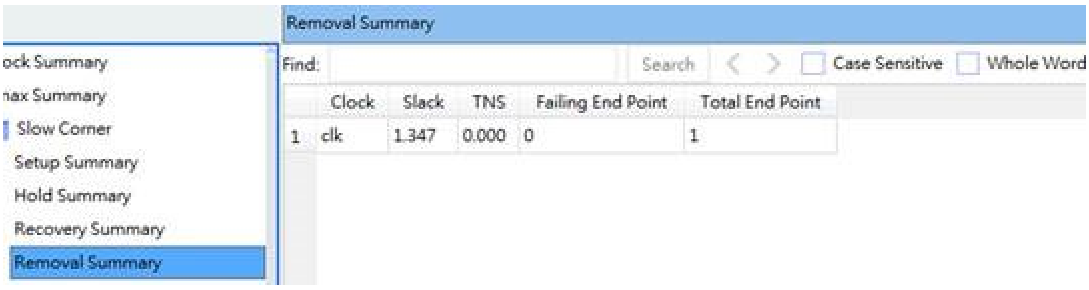


Figure 3-44 Removal Summary

o Minimum Pulse Width Summary

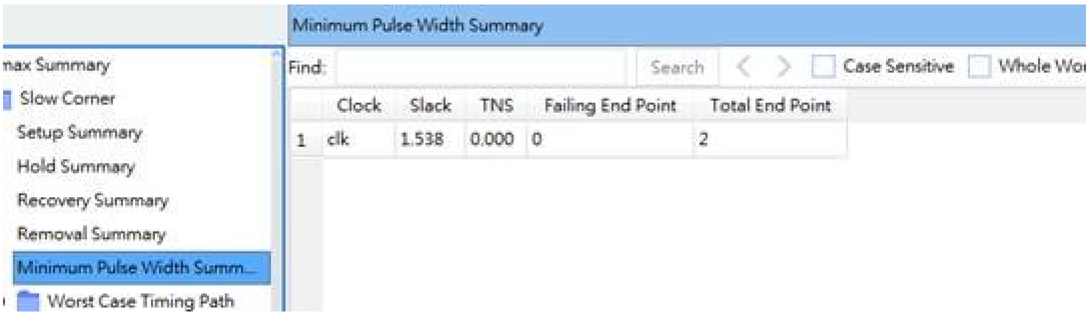
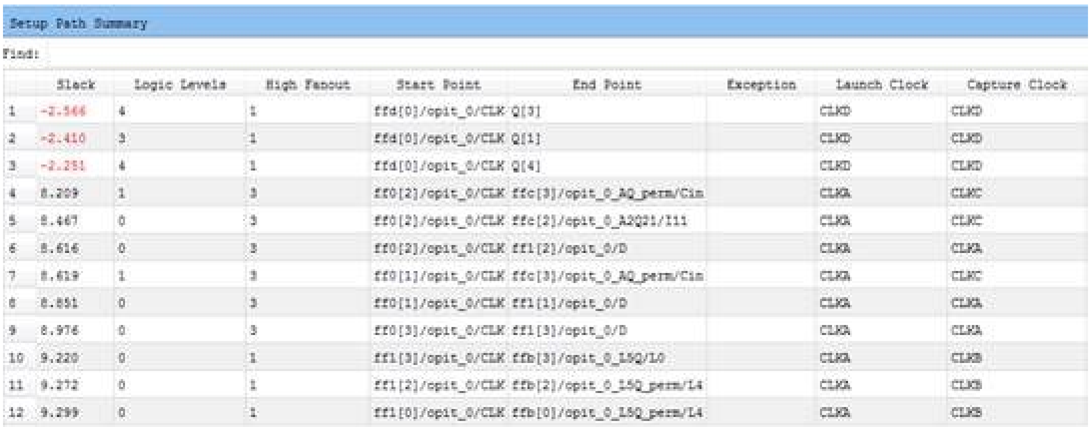


Figure 3-45 Minimum Pulse Width Summary

o Worst Case Timing path

Among them, the Worst Case timing path is divided into several types: Setup , Hold , Recovery , Removal , and Minimum Pulse Width . The summary information and detailed information of the corresponding path are listed in the report . Among them, the reports of Setup , Hold , Recovery , and Removal are similar, and the Path of Setup and Minimum Pulse Width is used as an example to illustrate, as shown in the figure below:



Setup Path Summary

Find:

	Slack	Logic Levels	High Fanout	Start Point	End Point	Exception	Launch Clock	Capture Clock
1	-2.566	4	1	ffd[0]/opit_0/CLK	Q[3]		CLKD	CLKD
2	-2.410	3	1	ffd[0]/opit_0/CLK	Q[1]		CLKD	CLKD
3	-2.251	4	1	ffd[0]/opit_0/CLK	Q[4]		CLKD	CLKD
4	8.209	1	3	ff0[2]/opit_0/CLK	ffc[3]/opit_0_AQ_perm/Cin		CLKA	CLKC
5	8.467	0	3	ff0[2]/opit_0/CLK	ffc[2]/opit_0_A2Q21/I11		CLKA	CLKC
6	8.616	0	3	ff0[2]/opit_0/CLK	ff1[2]/opit_0/D		CLKA	CLKA
7	8.619	1	3	ff0[1]/opit_0/CLK	ffc[3]/opit_0_AQ_perm/Cin		CLKA	CLKC
8	8.851	0	3	ff0[1]/opit_0/CLK	ff1[1]/opit_0/D		CLKA	CLKA
9	8.976	0	3	ff0[3]/opit_0/CLK	ff1[3]/opit_0/D		CLKA	CLKA
10	9.220	0	1	ff1[3]/opit_0/CLK	ffb[3]/opit_0_L5Q/L0		CLKA	CLKB
11	9.272	0	1	ff1[2]/opit_0/CLK	ffb[2]/opit_0_L5Q_perm/L4		CLKA	CLKB
12	9.299	0	1	ff1[0]/opit_0/CLK	ffb[0]/opit_0_L5Q_perm/L4		CLKA	CLKB

Figure 3-46 Setup Path Summary Report

Setup Path Summary in the figure above has the following information from left to right: Slack , Logic Levels , High Fanout , Start Point , End Point , Exception , Launch Clock , Capture Clock , Clock Edges , Clock Skew , Launch Clock Delay , Capture Clock Delay , Clock Pessimism Removal , Requirement , Data Delay , Logic Delay , Route Delay . In the Path Summary , the lines with slack less than 0 will be marked in red, and by default, they will be displayed in ascending order of slack . Below the Path Summary is the detailed information of the selected path , including whether the path meets the timing requirements, the data arrival time and required time of the path .

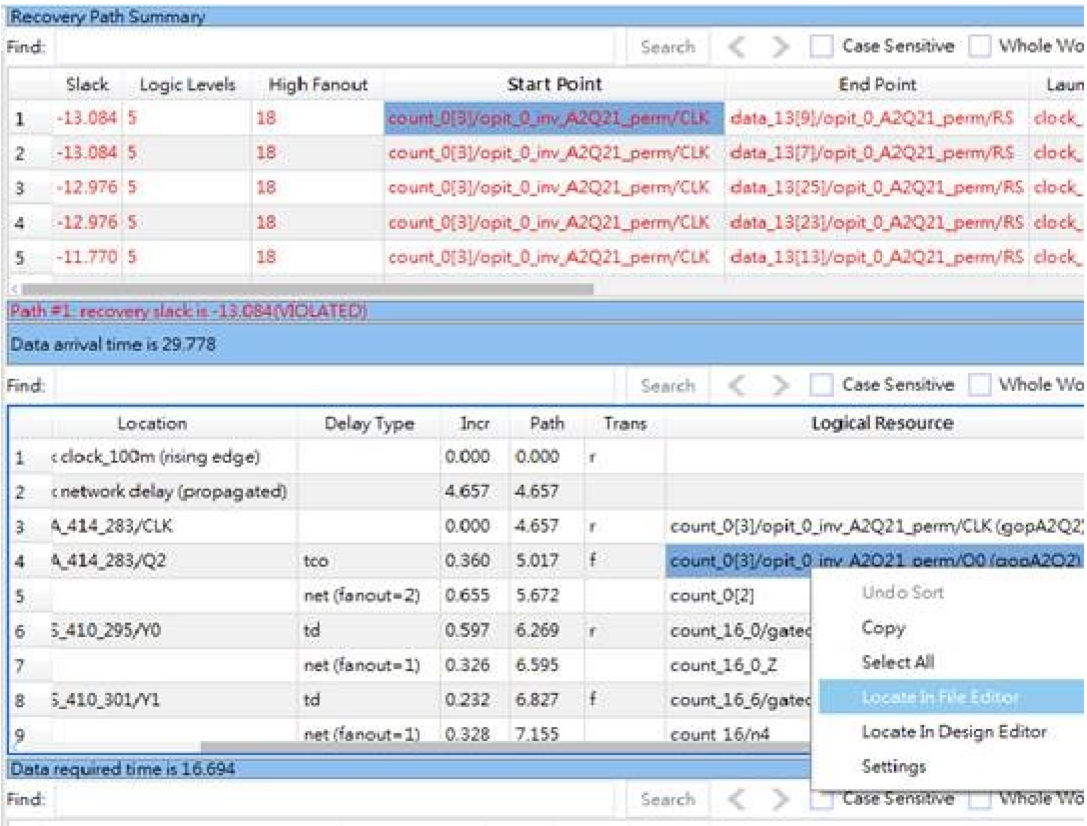


Figure 3-47 Detail timing Path Report

Start Point , End Point and the logical resource in the detailed path in the above figure can be right-clicked to jump to the corresponding RTL source file and DE to view.

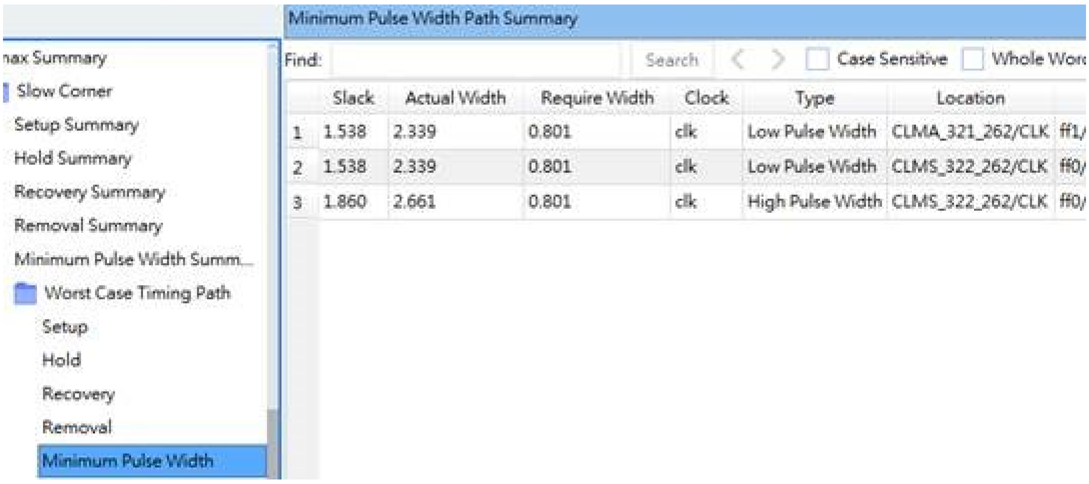


Figure 3-48 Minimum Pulse Width Path Report

Minimum Pulse Width Path Report is different from the Setup Path Report , all the information has been listed in the summary , no detailed information list is required, this information includes Slack , Actual Width , Required Width , Clock , Type , Location and Pin .

In addition, in the Flow Summary , you can also see whether the timing is violated. If the timing is satisfied, "All Constraints Met" will be displayed; if there is a timing that is not satisfied, the

specific unsatisfied items will be displayed (the red part in the figure below). Click to link to a detailed report. As shown below:



Figure 3-49 timing violation display

8. IO Datasheet

IO Datasheet mainly reflects the timing characteristics of IO, including :

o Input Ports Setup/Hold

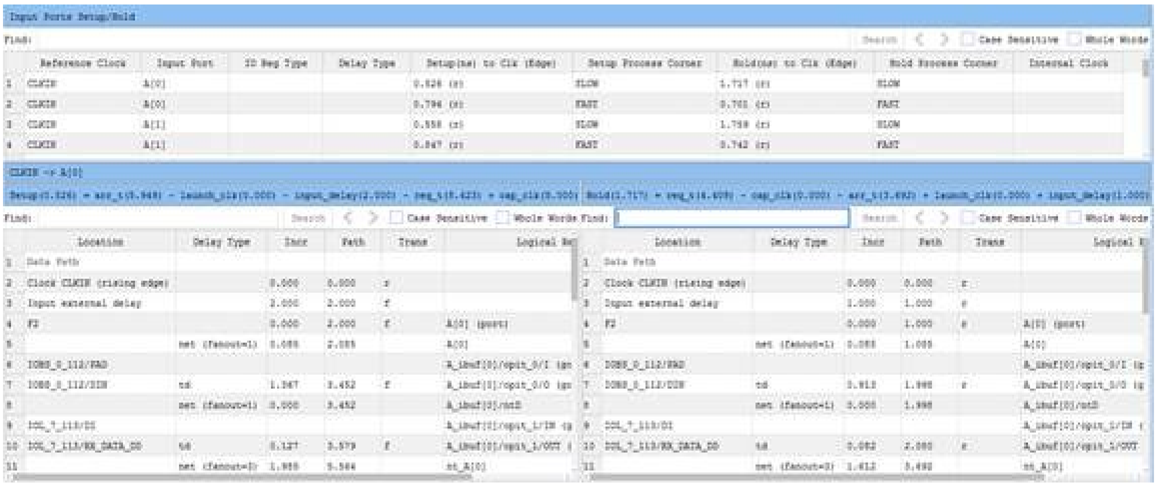


Figure 3-50 Input Ports Setup/Hold

If the Input Port is finally connected to a sequential unit, Input Ports Setup/Hold will report the Setup/Hold requirements of the Input Port by clock and corner . This requirement is to consider the Setup/Hold of the sequential unit and the Port and Clock ports connected to the sequential unit. Delay counts back.

o Output Ports Clock-to-out

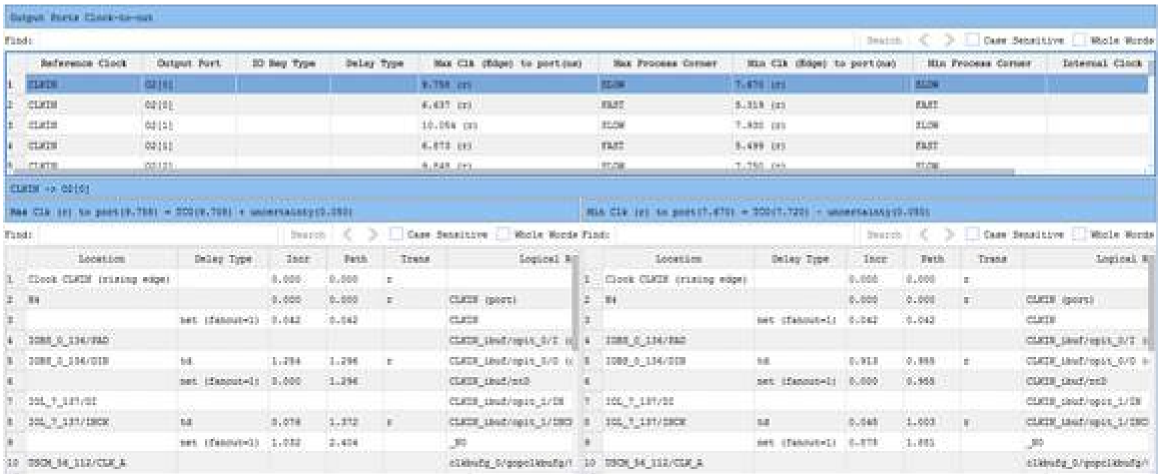


Figure 3-51 Output ports Clock-to-out

If the Output Port is connected from the sequential unit, Output ports Clock-to-out will report the Delay from the Clock Port connected to the sequential unit to the Output Port by clock .

o Combination Delays

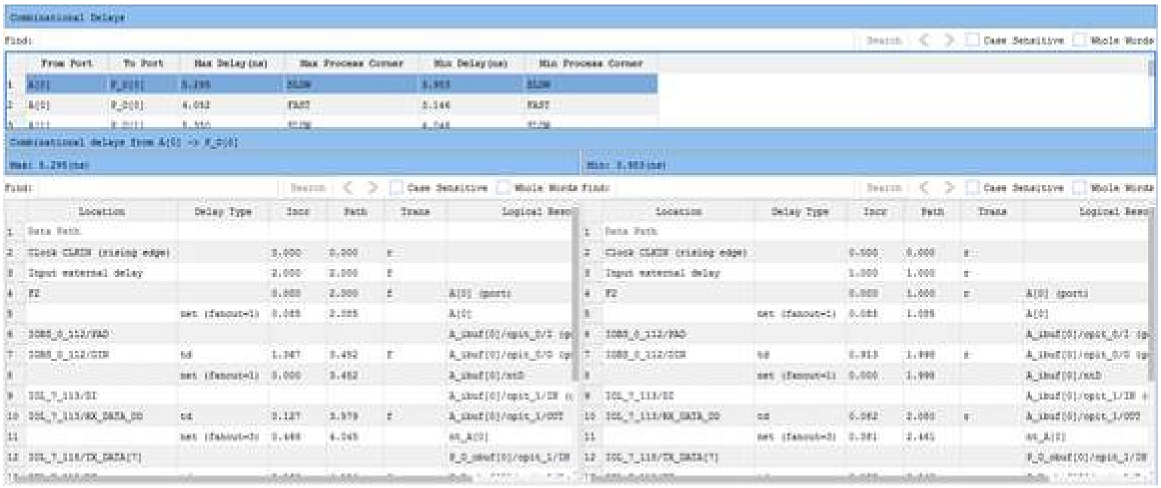


Figure 3-52 Combination Delays

If the Output Port is connected from the Input Port , Combination Delays will report the Delay from the Input Port to the Output Port .

o Setup/Hold times for input bus

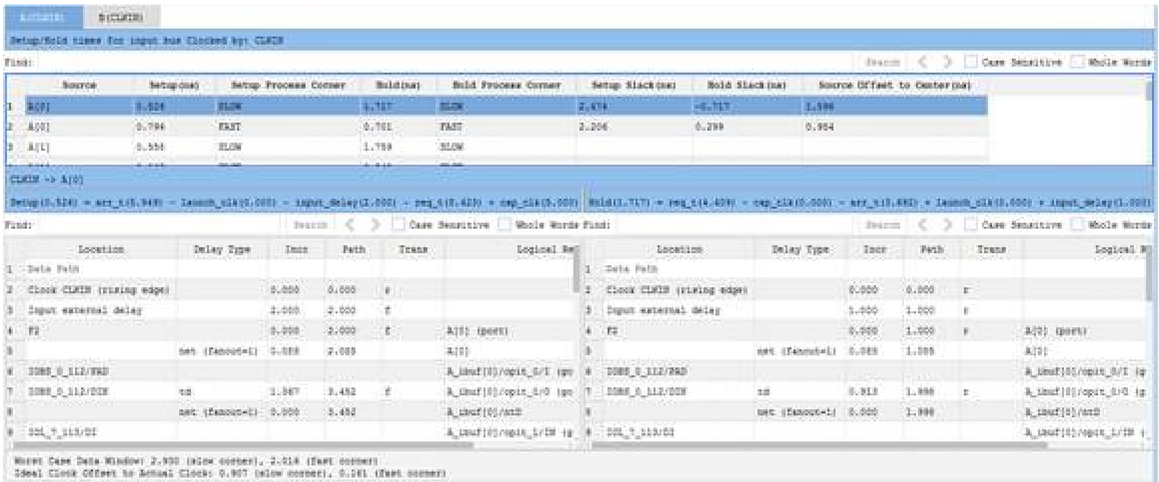


Figure 3-53 Setup/Hold times for input bus

Setup/Hold times for input bus is specifically for Input Buses to report Setup/Hold requirements, and calculate the worst case in Buses , and report the Slack of the port that has currently set timing constraints such as Input Delay and if the clock is to be located in the center of the data. Offset Delay (ie Source Offset to Center).

o Max/Min delays for output bus

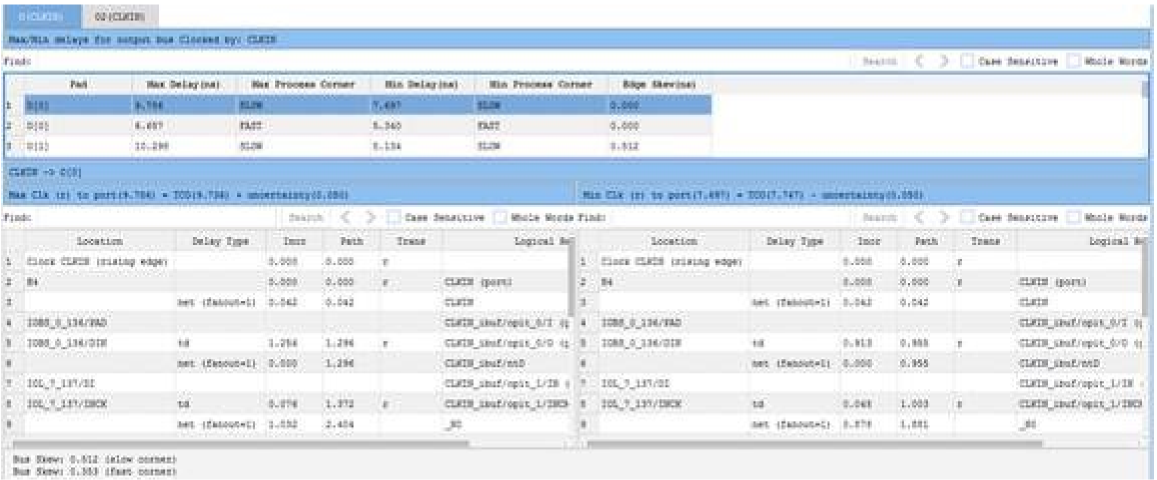


Figure 3-54 Max/Min delays for output bus

Max/Min delays for output bus is specifically for Output Buses to report the Delay requirements of Output Port , and calculate the worst delay , and select port 0 as a reference port to calculate the edge skew of other ports and this port .

9. Max Skew Report

Max Skew Report mainly reflects whether a set of timing paths constrained by set_max_skew meets the skew value of the constraint. The upper part of the window of the Max Skew report displays some summary information of the relevant paths . After a path is selected, the detailed information of the path will be displayed in the lower part of the report . If the slack value of the path is less than 0 , that is, if it is not satisfied, a red reminder will be displayed.

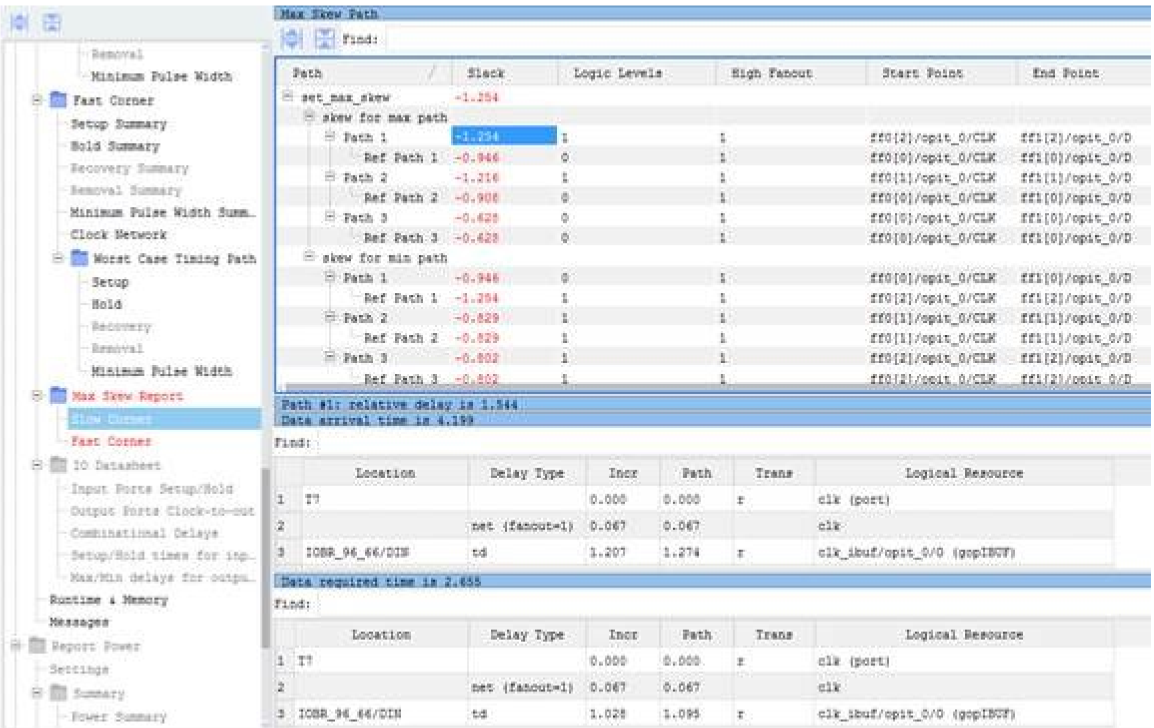


Figure 3-55 Max Skew Report

3.6 Report power

3.6.1 Report power setting

Report_Power_settings is introduced as follows. The option settings of Report Power are shown in the figure below:

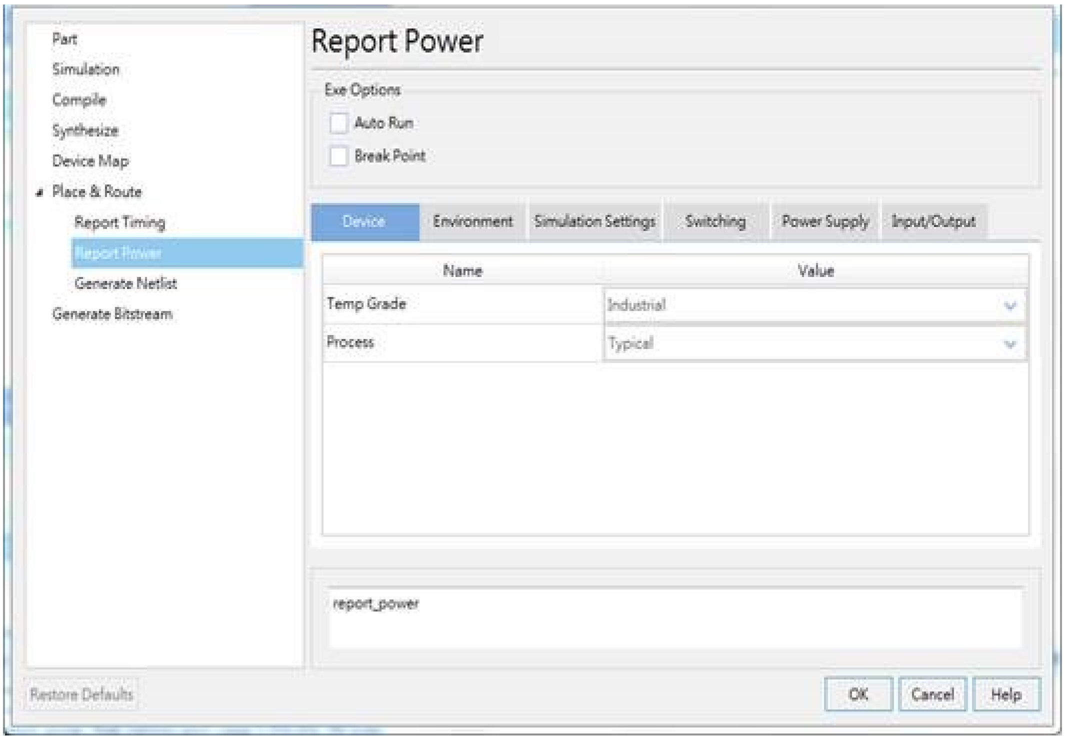


Figure 3-56 Report power option setting

There are two check boxes and six Tab pages in this window: Device , Environment , Simulation Settings , Switching , Power Supply and Input/Output .

(1) On the Device page, there are two device-related parameters that need to be selected by the user. The changed options will appear in the lower box, as follows:

Temp Grade : Temperature grade, including commercial grade Commercial and industrial grade Industrial , mainly affects the setting range of junction temperature and ambient temperature in Environment . The default is Industrial .

Process : Process deviation, including standard Typical and worst Worst , affects the final power consumption evaluation result. The default is Typical .

(2) On the Environment page, there are 9 environmental parameter configurations that need to be checked or specified by the user, which are:

Custom Junction Temperature : Whether the user specifies the junction temperature. After checking, except the Junction Temperature can be set, the rest cannot be modified. If unchecked, the default value is 25.000 . The default is unchecked.

Ambient Temperature: Ambient temperature, determined by the setting of Temp Grade in Device , specifically: Commercial (0~85) , Industrial (-40~100) . Default is 25.000 .

Junction Temperature : The default value is 25.000 , which is also determined by the setting of Temp Grade in Device , and the range is the same as the ambient temperature.

Custom Effective Theta JA : Whether the user specifies the thermal coefficient. After checking, the user can modify the default thermal coefficient. The default is unchecked.

Effective Theta JA : The equivalent thermal impedance that the heat generated by the chip spreads to the outside world, which is related to the process, packaging, and heat dissipation of the device. When Airflow (LFM) is Still , Heat-Sink is None , and Board Thermal Model is Normal , the default values of Effective Theta JA of each device are as follows:

Compact series:

PGC1KG-MBG256 , 30.3 ; PGC1KG-FBG256 , 29.3 ; PGC1KG-LPG144 , 31.0 ; PGC1KG-LPG100 , 31.73 ; PGC1KL-UWG36 , 27.4 ; PGC2KG-MBG256 , 30.3 ; PGC2KG-FBG256 , 29.3 ; PGC2KG-LPG144 , 31.0 ; PGC2KG- LPG100 , 31.73 ; PGC2KL-UWG49 , 27.4 ; PGC2KL-SSBG256 , 27.4 ; PGC4KD-MBG256 , 25.7 ; PGC4KD-LPG144 , 30.1 ; PGC4KD-MBG324 , 24.9 ; PGC4KD-MBG332 , 24.2 ; PGC4KD-FBG256 , 25.5 ; PGC4KL-SSBG256 , 21.6 ; PGC4KL-UWG81 , 21.6 ; PGC4KLS-SBG81 , 21.6 ; PGC7KD-FBG484 , 19.7 ; PGC7KD-MBG400 , 22 ; PGC7KD-MBG332 , 23.2 ; PGC7KD-MBG256 , 21.8 ; PGC7KD-LPG144 , 28.9 ; PGC10KD-MBG400 , 21.0 ; PGC10KD-MBG484 , 19.6 ; PGC10KD-MBG256 , 20.8

PGL series:

PGL12G-FBG256 , 30.7 ; PGL12G-LPG144 , 29.7 ; PGL22G-FBG256 , 20.7 ; PGL22G-MBG324 , 21.2 ; PGL22GS-LPG176 , 21.8 ; PGL25G-FBG256 , 19.8 ; PGL25G-MBG324 , 18.1 ; PGL25G-FBG484 , 17.8 ; PGL50G- FBG484 , 16.7 ; PGL50G-MBG324 , 16.7 ; PGL50G-MBG484 , 16.7 ; PGL50H-FBG484 , 16.7 ; PGL50H- MBG324 , 16.7 ; PGL50H - MBG484 , 16.7 ;

PG2L series:

PG2L25H-MBG325 , 21.2 ; PG2L25H-SBG238 , 21.2 ; PG2L100H-FBG676 , 12.5 ; PG2L100H-FBG484 , 15.2 ; PG2L100H-MBG324 , 17

PGT series:

PGT30G-FFBG484 , 10.59 ; PGT180H-FFBG1152 , 7.06 ; PGT180H-FFBG1140 , 7.06 ; PGT180H-FFBG676 , 7.58

PG2T series:

PG2T390H-FFBG676 , 9.9 ; PG2T390H-FFBG900 , 9.7

Airflow(LFM) : Airflow conditions, there are four options : Still , Low , Medium and High . The default is Still .

Heat-Sink : Heat dissipation, there are five options : None , Custom , Low , Medium and High . Defaults to None .

Effective Theta SA : Heat dissipation thermal resistance coefficient, which can be modified when Heat-Sink is selected as Custom , and the rest cannot be modified. Default is empty.

Board Thermal Model : The heat dissipation of the board, there are four options : JEDC , Best , Normal , and Worst . The default is Normal .

(3) Simulation Settings simulation waveform setting page:

Specify Input VCD File: The user-specified post-simulation file, which records the simulation waveform, through which the signal inversion can be obtained. Default is empty.

(4) Switching : There are 12 parameter values that need to be set by the user in the signal-related parameter configuration interface , which are:

Output Load (pF) : IO external load and other capacitance, the value is [0~50] , the default is 5.000 ;

Default Clock Freq (MHz) : The default clock frequency [0~500] , the default is 100.000 ;

Default Toggle Rate : The default toggle rate [0~1] , the default is 0.125 ;

Default Static Probability : The default static high level probability [0~1] , the default is 0.125 ;

Default I/O Toggle Rate : The default toggle rate of I/O [0~1] , the default is 0.125 ;

Default I/O Enable Probability : The default enable probability of I/O [0~1] , the default is 0.500 ;

Default BRAM Toggle Rate : The default toggle rate of DRM [0~1] , the default is 0.125 ;

Default BRAM Enable Probability : The default enable probability of DRM [0~1] , the default is 1.000 ;

Default APM Toggle Rate : APM 's default toggle rate [0~1] , the default is 0.125 ;

Default APM Enable Probability : The default enable probability of APM [0~1] , the default is 1.000 ;

Default HSST Toggle Rate : The default toggle rate of HSST [0~1] , the default is 0.125 ;

Default HSST Enable Probability : The default enable probability of HSST [0~1] , the default is 0.500 .

(5) Power Supply : The main power supply voltage setting interface includes 7 voltage values, which are:

Core VCC (compact series voltage range is [2.25-3.64] , PGL , PGT series voltage range is [0.99-1.21] , PG2L , PG2T series voltage range is [0.95-1.05]), PGC series default is 3.300 , PGL , PGT series The default is 1.100 for the series , and 1.000 for the PG2L and PG2T series ;

Bank VCCIO3.3 voltage [2.97-3.63] , the default is 3.300 ;

Bank VCCIO2.5 voltage [2.25-2.75] , the default is 2.500 ;

Bank VCCIO1.8 voltage [1.62-1.98] , the default is 1.800 ;

Bank VCCIO1.5 voltage [1.35-1.65] , the default is 1.500 ;

Bank VCCIO1.2 voltage [1.08 - 1.32] , the default is 1.200 ;

Auxiliary power supply VCCAUX (PGC series does not support, PGL , PGT series voltage range is [2.97-3.63] , PG2L , PG2T series voltage range is [1.71-1.89]) , PGL , PGT series default is 3.300 , PG2L , PG2T series default is 1.800 .

(6) Input/Output : The input and output setting interface mainly selects the import configuration file and output power consumption file path. Contains three items:

Output power report file : Power consumption report output file, the default is empty;

Output Fast settings file : The power consumption report settings file of the project, which is empty by default;

Output PPF file : the power consumption evaluation file output to PPP , the default is empty;

3.6.2 Report PowerReport

Double-click or right- >Run to run Report Power will display the corresponding report. As shown below:

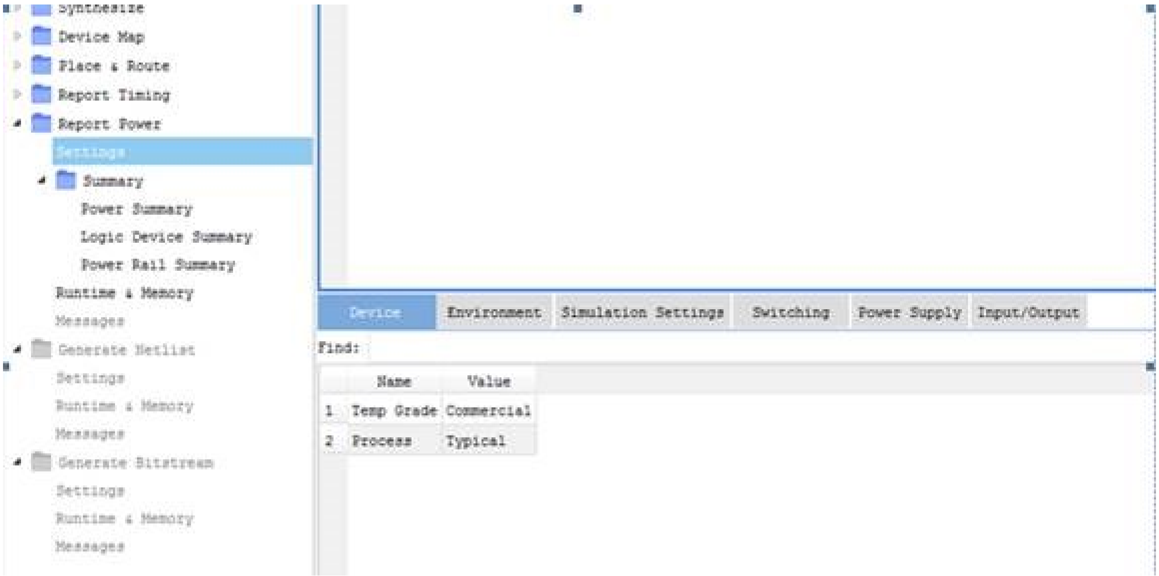


Figure 3-57 Report power report

In the Reports Summary , you can see the setting information and power consumption information of the power consumption report. The setting information includes:

3) Settings

Settings is mainly Design -related information, such as the top -level module name, the VCD file of the signal data for calculating power consumption, etc.

4) Device Settings

Device Settings is the information of the device, mainly including device type, series, package, temperature, speed grade and process deviation.

5) Environment

Environment is set to the environmental parameters of the power consumption report, including temperature, junction temperature, thermal resistance, etc.

6) Power Rail

Power Rail sets the voltage value of each power supply in the chip in the calculation of power consumption, such as vcc , vccio and so on.

7) Default Activity Rate

Default Activity Rate sets the default values of the signal transmission rate, flip condition, and port enable probability of each resource during the power consumption calculation process.

Power consumption information includes:

1) Power Summary

Power Summary reports the overall power consumption and junction temperature of the design under the current settings, mainly including the total on-chip power consumption, static power consumption, and chip junction temperature.

2) Logic Device Summary

Logic Device Summary reports the dynamic power consumption of each main resource and the percentage of the total power consumption according to the resource usage classification in the design .

3) Power Rail Summary

Power Rail Summary reports power consumption according to the power consumption of each power supply in the chip, mainly including power supply name, voltage value (unit V), current value (unit A), external current value (unit A) and on-chip power consumption (unit W) .

3.7 Generate Netlist

Generate_Netlist_settings runs Generate Netlist to generate the post-layout simulation netlist file sim.v and the timing back-annotation file sdf .

The post-imitation library directory is $InstallDir\arch\vendor\pango\verilog\bsim , such as C:\pango\PDS_2021.3\arch\vendor\pango\verilog\bsim .

Generate Netlist are shown in the figure below:

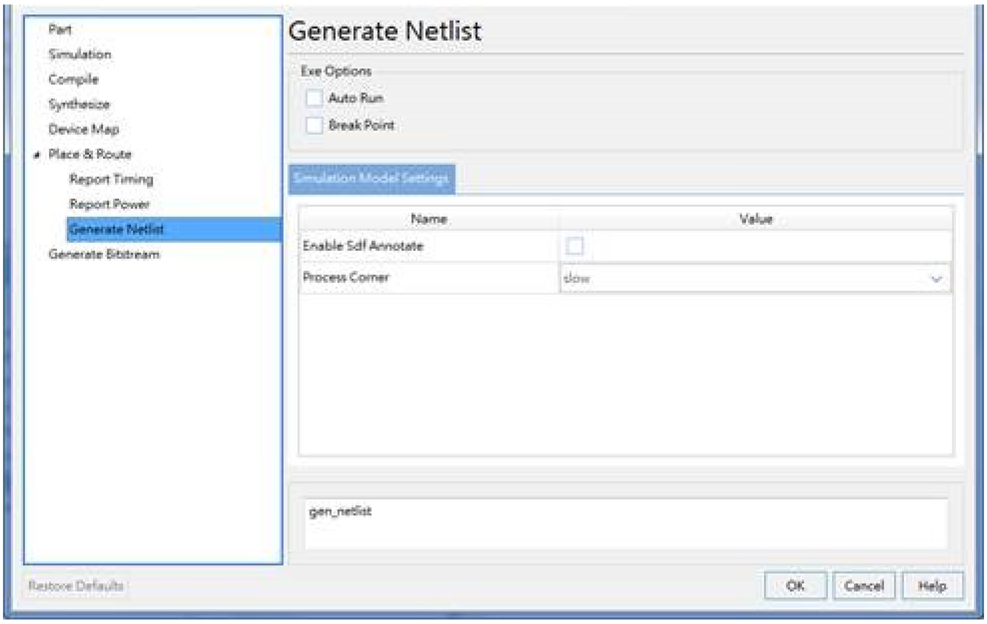


Figure 3-58 Generate Netlist option settings

Simulation Model settings

【 Enable Sdf Annotate 】 Select whether to generate the sdf_annotate task statement in the simulation netlist (sim.v) .

【 Process Corner 】 Specify the process corner (slow or fast) corresponding to the sdf delay file .

3.8 Design Editor

By executing Place & Route , you can open Design Editor through Design Editor in Tools . For the usage of Design Editor , please refer to "Design_Editor_User_Guide ".

3.9 Generate Bitstream

Generate_Bitstream_settings generates a binary bitstream file, which is the last step in Pango Design Suite design.

Generate Bitstream option settings As shown below:

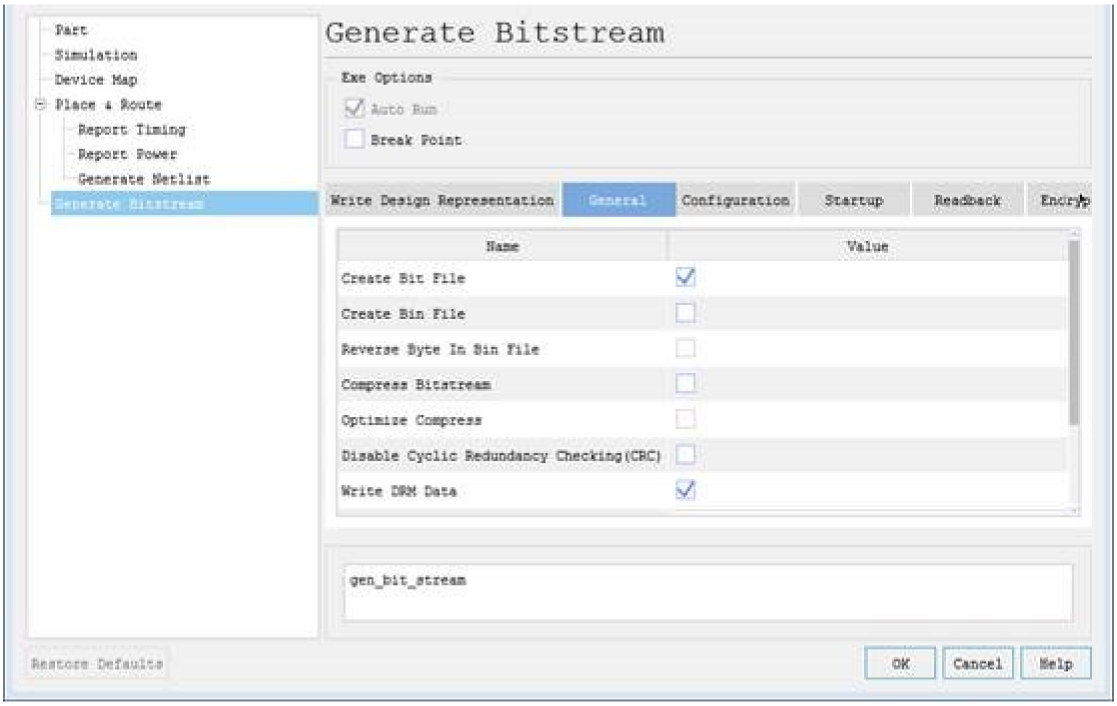


Figure 3-59 Generate Bitstream option settings

Generate Bitstream configuration option: The content of the bitstream configuration option is related to the specific chip. The above figure shows the bitstream configuration option of PGL50H .

General

【 Create Bit File 】 Choose whether to generate a bit file, select Yes to generate an sbit file, select No to not generate, the default value is Yes

【 Create Bin File 】 Choose whether to generate a bit file without information header. If Create bit file is configured as Yes , check it to generate a bin file without information header. If you do not select it, it will not be generated. The default is unchecked

【 Reverse Bit In a Byte 】 Choose whether to reverse the high order and low order of each Byte in the bin file . After checking, reverse the order of bit7...bit0 to bit0...bit7 . It is not checked by default.

[Reverse Byte In a Word] Choose whether to reverse the high and low bits of each Word (one word = 4 bytes) in the bin file, and reverse byte3byte2...byte0 to byte0...byte2byte3 after checking . By default, it is not checked

【 Compress Bitstream 】 Choose whether to compress the bitstream file. Under the premise that Create bit file is configured as Yes , select Yes to generate a compressed sbit file, and select No to generate an uncompressed sbit file. The default value is No

[Optimize Compress] Choose whether to optimize the compressed bit stream. The meaning of optimized compression is that when the frame data is 0 , it will not be written into the compressed bit stream file. When the user chooses to compress the bit stream, the default value of optimized compression is related to the device.

【 Disable Cyclic Redundancy Checking (CRC) 】 Select whether to ignore CRC verification. The default is to perform CRC verification

【 Write DRM Data 】 Select whether to write DRM data, the default value is Yes .

[Unused IO Status] Select the status of unused IO. The default value of different series is different. The default value of PGT180H and PGT200H is PULLUP , the default value of Compact and Logos series is PULLDOWN, and the default value of Logos2 , Titan2 , Titan3 and Titan3e series is UNUSED .

【 Show Time Info 】 Select whether to display the time and date in the header information of the bit stream. It is checked by default. This option does not affect the user design function.

【 Show Manufacturer Info 】 Choose whether to display the manufacturer in the header information of the bit stream. It is checked by default. This option does not affect the user design function.

Configuration

【 Usercode 】 Assign a value to the user identification register, input 8 -digit hexadecimal user code , the value will be written into the bit stream file, the default value is 0xFFFFFFFF

【 Set Configuration Bank Voltage(SCBV) 】 Set the voltage of the configuration bank , the default is None (this option is only supported in PG2L100H).

[Master Configuration Clock Frequency] Master mode clock clk frequency selection, the default value of Titan series is 12.5M , the default value of Logos series is 3.125M , the default value of Compact series is 2.08M, and the default value of Logos2 and Titan2 series is 2.99M .

【 System Clock Frequency 】 Configure memory clock mclk frequency selection, the default value of PGL series is 100M , and the default value of Titan series is 50M . (This option is only supported in PGL and Titan series)

[Enable OSC Shut Off] Control whether to allow the user logic to shut down the OSC , the default value is not allowed (PGT30 this setting is invalid)

【 Enable Watchdog In User Mode 】 Select whether to enable the watchdog in user mode, the default is not enabled.

【 Enable Watchdog In Configuration Mode 】 Select whether to enable the watchdog in configuration mode, the default is not enabled.

[Load Watchdog] Set the timeout time of the watchdog, the default is 3FFF_FFFF

【 Enable Version Select(VS) Pin 】 Enable the version control pin, which is disabled by default

【 Enable Version Fallback 】 Select whether to enable version fallback, the default is enabled

【 Version Fallback Control 】 Select the fallback bit stream version, you can choose " golden bit stream " or "Last Used bit stream" , the default is golden bit stream

【 Enable RS Pin 】 Select whether to enable the RS 【 1:0 】 pin output, which is not enabled by default.

【 RS Pin Value 】 Set RS Pin Value , the range is 0~3 , the default value is 0

[Set Fallback Retry Times] Set the number of version fallback attempts, the default is 1

【 Set Bitstream Retry Times 】 Set the number of bitstream retry times, the default is 0

[RST_N pin] Select whether the RST pin is pulled up or suspended, and the default is pulled up

[TDI Pin] Select whether the TDI pin is pulled up or suspended, and the default is pulled up

[TMS Pin] Select whether the TMS pin is pulled up or suspended, and the default is pulled up

[TCK Pin] Select whether the TCK pin is pulled up or suspended, and the default is pull up

[TDO Pin] Select whether the TDO pin is pulled up or suspended, and the default is pulled up

[INIT_FLAG_N pin] Select whether the INIT_FLAG_N pin is pulled up or suspended, and the default is pulled up

[CFG_DONE Pin] Select whether the CFG_DONE pin is pulled up or suspended, and the default is pulled up

[CFG_CLK Pin] Select the pull-up or floating of the CFG_CLK pin, the default is pull-up

[MODE_2 Pin] Select whether the MODE_2 pin is pulled up or suspended, and the default is pull up

[MODE_1 Pin] Select whether the MODE_1 pin is pulled up or suspended, and the default is pull up

[MODE_0 Pin] Select whether the MODE_0 pin is pulled up or suspended, and the default is pull up

[Enable External Master Configuration Clock] Select whether to enable the external master configuration clock, the default is not enabled

[BPI Read Cycle] Select the BPI read cycle, the default is 1

【 BPI Page Size 】 Select the page size of BPI , the default is 1 Byte/Half Word

【 BPI Mode 】 Select the BPI mode, the default is asynchronous

[Enable Done Synchronization] Select whether the Done signal is synchronized, the default is not synchronized

【 SRAM Retention 】 Enable SRAM retention test, unchecked by default

[Over Temperature Shut Off] Enable over temperature shutdown, unchecked by default

Startup

[Wake Up Time Slot Length] Wake up cycle length selection, that is , the time interval between T1 , T2 , T3 , the default value is 1 , which refers to a wake up clock cycle

[Done Time Slot] Select the time when the done signal is pulled high, the default value is T1

[Gwen Time Slot] Select the time when the gwen signal is pulled high, the default value is T3

[Grsn Time Slot] Select the time when the grsn signal is pulled high, the default value is T4

[Gouten Time Slot] Select the time when the gouten signal is pulled high, the default value is T2

【 Enable Wait DCI Match 】 Wake up and wait for DCI match, the default value is not to wait

[Enable Wait PLL Lock] Wait for PLL when waking up , the default value is not waiting

[Wake Up Clock] Select the wake-up clock, the default is the main configuration clock

[Enable USER Clock Wake Up] Whether to use the user clock to wake up, the default is not checked

Read back

【 Create Mask File 】 Choose whether to generate a mask file to determine the comparison rules between the readback file and the original file. Select Yes to generate a mask file, select No to not generate, the default value is Yes

[Persist Slave Parallel Pins] Controls whether the external parallel port is reserved for readback after the parallel mode configuration is completed, and it is not reserved by default. (Titan family device option)

[Persist Ipal] After the control configuration is completed, whether the internal parallel port is reserved for readback, the default is reserved (only valid for PGT30G settings)

[Disable Readback CRC] Select whether to enable CRC verification during readback, and enable readback CRC verification by default

【 Bitstream Security 】 Control reconfiguration and readback configuration memory function, the default value is to allow reconfiguration and allow readback

[Select Persist Pin] drop-down box to select Persist Slave Parallel Pins or Persist Slave SPI Pins or None , the default is None .

【 Master Configuration Clock Frequency In Read Back 】 Readback clock selection, the default value is 2.08M

【 Enable CRC Clock In Read Back 】 Enable readback CRC clock, the default value is unchecked

【 Enable Mask Variable Memory In Read Back 】 Select whether to mask the RAM area when reading back, and the default is to mask the RAM area.

【 Persist Pin 】 Select to reserve the multiplexed port for configuring the interface or release it to the user. The default is to release the port.

Encryption

[Encrypt Bitstream] Check whether to encrypt the bit stream file. Under the premise that Create bit file is configured as Yes , check it to generate encrypted sbit files and nky files (including the 128 -bit initial CBC value and 256 -bit encryption required for encryption). Key), if unchecked, an unencrypted sbit file will be generated, and the default value is unchecked. The user can edit the CBC and key string or select the nky file, if the user does not specify, the nky file will be randomly generated

【 Select Key Type 】 Configure whether to use the internal KEY , the default value is Key . When Temporary Key is selected , the corresponding nky file needs to be downloaded before downloading the bit stream each time. If Key is selected , the key is first burned to the efuse module

of the chip (this operation is only performed once), and then the bit stream can be directly downloaded

[Starting CBC Value] The user manually enters the initial CBC string, the characters are in hexadecimal , the input length is up to 32 characters, and the default is empty

[Starting GCM Value] The user manually enters the initial GCM string, the characters are in hexadecimal , the input length is up to 24 characters, and the default is empty

【 Input Encryption Key File 】 Select the nky file, if the key file is selected here, the software chooses to use the key file for encryption, regardless of whether the user has entered the key string in the option, the default is empty.

[Key String] The user manually enters the key string, the characters are hexadecimal characters, the input length is up to 64 characters, and the default is empty

【 Number of Encryption Block 】 The block number of block encrypted data, the characters are decimal characters, the input range is 0~131071 , the default value is 0

【 Enable Obfuscate 】 Enable obfuscated encryption, used in conjunction with the encryption function , disabled by default

【 Enable Self Authentication 】 Enable the self-authentication function and perform self-authentication on encrypted data, which is disabled by default

【 Enable DPA 】 Enable the DPA protection function, used in conjunction with the encryption function, the default is not enabled

[DPA Protect Region] Set the DPA protection region, the default is ALL

【 Data Width 】 Encrypted data width setting, the data bit width used when configuring encrypted data, the default value is X1

Authentication

【 Authenticate Bitstream 】 Choose whether to perform RSA-2048 authentication bitstream file, the default is no authentication

[Input RSAPrivate Key File] Select the private key file (pem file) for RSA-2048 authentication . If the user chooses to authenticate the data flow without specifying the private key file, the private key file will be randomly generated. The default is empty

Notes on Logos2 encryption:

a) Does not support DPA protection for compressed data streams (when compression is checked, Enable DPA cannot be checked)

b) Compressed data streams and DPA -protected data streams do not support block encryption (Number of Encryption Blocks must be 0 when compressing data streams or DPA -protected data streams)

c) Enable Self Authentication and Enable DPA cannot be checked at the same time

d) Enable DPA is checked, Authenticate Bitstream, Encrypt Bitstream must be checked

e) When Enable Self Authentication is checked, block encryption is not supported.

f) When Number of Encryption Blocks is not 0 , Encrypt Bitstream must be checked

SEU File

【 Soft Error Insertion 】 The soft error insertion file generation configuration used for SEU verification, the error insertion position can be selected as Random , Unused area.

Feature Control

【 Feature Value 】 Displays the corresponding feature control value (hexadecimal) after the selected feature control bit.

Currently only supports PGC series, as shown in the figure 3-60 shows the option interface of the feature control bit.

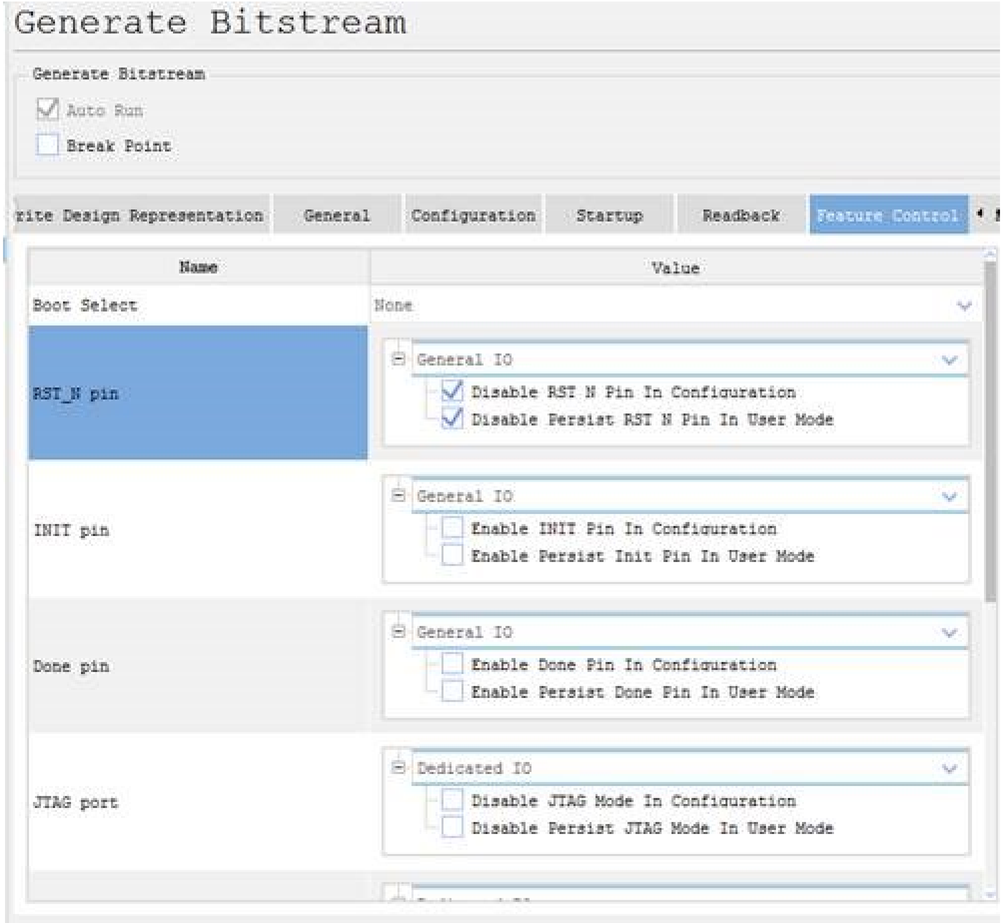


Figure 3-60 Option interface of feature control bits

The following table shows the support of the functions of the compact series feature control bits :

name	Status	value	Description
Boot Select	\	Master Auto Mode (from embed flash)\ (default) Master SPI Mode(from outer SPI flash)\None	Select the boot mode, and only when the main and self-loading is selected can the main and self-loading dual boot be set; when it is not None , the normal dual-boot can be set
RST_N pin	General IO (default)	Check Disable RST_N Pin In Configuration and Disable persist RST_N Pin in User Mode	RST_N pin is disabled in both user mode and configuration mode
	Dedicated IO	Uncheck Disable RST_N Pin In Configuration and Disable persist RST_N Pin in User Mode	Enable the RST_N pin in both user mode and configuration mode
	Other Usage	Any combination of options can be set to Other Usage	Disable or enable the INIT pin according to the actual option
INIT pin	General IO (default)	Uncheck Enable INIT Pin In Configuration and Enable persist INIT Pin in User Mode	INIT pin is disabled in both user mode and configuration mode
	Dedicated IO	Check Enable INIT Pin In Configuration and Enable persist INIT Pin in User Mode	INIT pin in both user mode and configuration mode
	Other Usage	Any combination of options can be set to Other Usage	Disable or enable the INIT pin according to the actual option
Done pin	General IO (default)	Uncheck Enable Done Pin In Configuration and Enable persist Done Pin in User Mode	Done pin is disabled in both user mode and configuration mode
	Dedicated IO	Check Enable Done Pin In Configuration and Enable persist Done Pin in User Mode	Enable the Done pin in both user mode and configuration mode

	Other Usage	Any combination of options can be set to Other Usage	Disable or enable the Done pin according to the actual option
Jtag port	General IO	Check Disable Jtag Mode In Configuration and Disable persist Jtag Mode in User Mode	the Jtag interface in both user mode and configuration mode
	Dedicated IO (default)	Uncheck Disable Jtag Mode In Configuration and Disable persist Jtag Mode in User Mode	Jtag interface in both user mode and configuration mode
	Other Usage	Any combination of options can be set to Other Usage	Jtag interface according to the actual options
Slave SPI port	General IO	Check Disable Slave SPI Mode In Configuration and Disable persist Slave SPI Mode in User Mode	the slave SPI interface in both user mode and configuration mode
	Dedicated IO (default)	Uncheck Disable Slave SPI Mode In Configuration and Disable persist Slave SPI Mode in User Mode	SPI interface in both user mode and configuration mode
	Other Usage	Any combination of options can be set to Other Usage	Disable or enable slave SPI interface according to actual options
Slave I2C port	General IO	Check Disable Slave I2C Mode In Configuration and Disable persist Slave I2C Mode in User Mode	the slave I2C interface in both user mode and configuration mode
	Dedicated IO (default)	Uncheck Disable Slave I2C Mode In Configuration and Disable persist Slave I2C Mode in User Mode	slave I2C interface in both user mode and configuration mode
	Other Usage	Any combination of options can be set to Other Usage	Disable or enable the I2C interface according to the actual option
I2C Address	\	The default value is 0	I2C address
Dual Boot Mode	\	Disable (default) /Dual boot	Whether to choose dual boot mode
advance	\	Disable Slave Parallel Mode In Configuration (checked by default)	Whether to disable slave parallel interface in configuration mode
		Enable Fast Master SPI Mode (unchecked by default)	Whether to enable the master SPI interface
		Disable Persist Slave Parallel Mode In User Mode (checked by default)	Whether to disable slave parallel interface in user mode
		Enable Master SPI Mode In User Mode (unchecked by default)	SPI interface in user mode
		Enable Slowly Read Mode (unchecked by default)	Whether to enable slow read mode
Features	\	Default is 2090	characteristic control value

Table 3-1 PGC series support

The functions supported by different devices are different. The following table shows the support of functions other than Feature Control :

type	configuration item	PGT30G	PGT180H	PGL series	PGC series	Logos2, Titan2 series
General	Create Bit File	√	√	√	√	√
	Create Bin File	√	√	√	√	√
	Reverse Bit In a Byte	√	√	√	√	√

	Reverse Byte In a Word	√	√	√	√	√
	Compress Bitstream	√	√	√	√	√
	Optimize Compress	x	x	√	√	√
	Disable CRC	x	x	√	√	√
	Write DRM Data	x	x	√	√	√
	Unused IO Status	√	√	√	√	√
Configuration	Usercode	√	√	√	√	√
	Set Configuration Bank Voltage (SCBV)	x	x	x	x	√
	Master Configuration Clock Frequency	√	√	√	√	√
	System Clock Frequency	√	√	√	x	x
	Enable OSC Shut Off	x	√	√	√	√
	Enable Watchdog In Configuration Mode	x	x	√	√	√
	Load Watchdog	x	x	√	√	√
	Enable Done Synchronization	x	x	√	√	√
	Enable Version Select(VS) Pin	x	x	√	x	√
	Enable RS Pin	x	x	x	x	√
	RS Pin Value	x	x	x	x	√
	Enable Version Fallback	x	x	x	x	√
	Version Fallback Control	x	x	√	x	√
	Set Fallback Retry Times	x	x	√	x	x
	Set Bitstream Retry Times	x	x	√	x	x
	RST_N pin	x	x	√	x	√
	TDI Pin	x	x	√	x	√
	TMS Pin	x	x	√	x	√
	TCK Pin	x	x	√	x	√
	TDO Pin	x	x	√	x	√
	INIT_FLAG_N pin	x	x	x	x	√
	CFG_DONE pin	x	x	x	x	√
	CFG_CLK pin	x	x	x	x	√
	MODE_2 pin	x	x	x	x	√
	MODE_1 pin	x	x	x	x	√
	MODE_0 pin	x	x	x	x	√
	Enable External Master Configuration Clock	x	x	√	x	√
	BPI Read Cycle	x	x	√	x	√
	BPI Page Size	x	x	√	x	√
	BPI Mode	x	x	√	x	√
	SRAM Retention	x	x	x	√	x
Startup	Wake Up Time Slot Length	√	√	√	x	√

	Done Time Slot	√	√	√	x	√
	Gwen Time Slot	√	√	√	x	√
	Grsn Time Slot	√	√	√	x	√
	Gouten Time Slot	√	√	√	x	√
	Enable Wait PLL Lock	√	√	√	√	√
	Enable Wait DCI Match	x	x	√	x	x
	Wake Up Clock	x	x	√	√	x
	Enable USER Clock Wake Up	x	x	x	x	√
ReadBack	Create Mask File	√	√	√	√	√
	Persist Slave Parallel Pins	√	√	√	x	x
	Bitstream Security	√	√	√	√	√
	Disable Readback CRC	x	x	√	√	√
	Persist Slave SPI Pin	x	x	√	x	x
	Enable CRC Clock In Read Back	x	x	x	√	x
	Master Configuration Clock Frequency In Read Back	x	x	x	√	x
	Persist Ipal	√	x	x	x	x
	Enable Mask Variable Memory In Read Back	x	x	√	x	√
Encryption	Encrypt Bitstream					√
	Select Key Type					√
	Starting CBC Value					x
	Input Encryption Key File	√	√	√	x	√
	Key String					√
	Stratting GCM Value	x	x	x	x	√
	Number of Encryption Blocks	x	x	x	x	√
	Enable Obfuscate	x	x	x	x	√
	Enable Self Authentication	x	x	x	x	√
	Enable DPA	x	x	x	x	√
	Data Width	x	x	x	x	√
Authentication	Authenticate Bitstream	x	x	x	x	√
	Input RSAPrivate Key File	x	x	x	x	√

Table 3-2 Other function support

PGC series in the above table include PGC1KG, PGC1KL, PGC2KG, PGC2KL, PGC4KD, PGC4KL, PGC7KD and PGC10KD .

Run Generate Bitstream to generate a bitstream file, you can see the interface as follows:

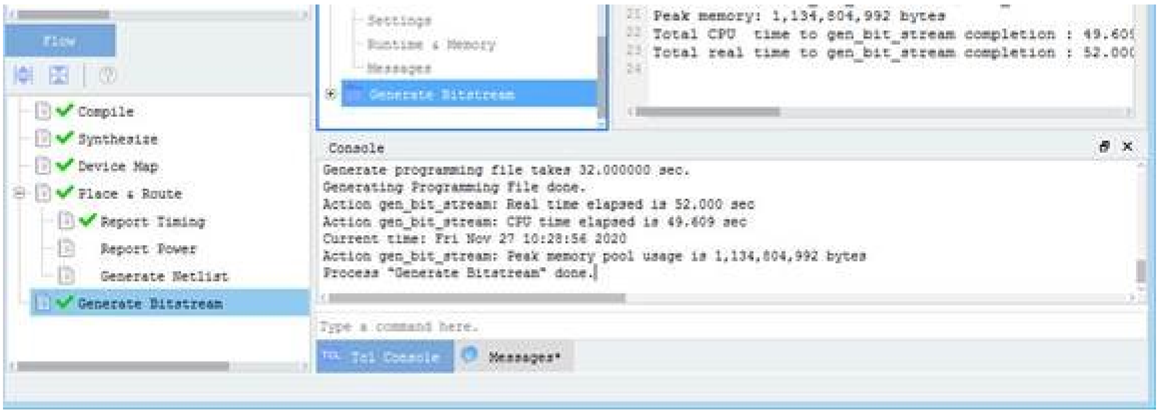


Figure 3-61 Software interface after running Generate Bitstream

After generating the .sbit bit stream file, check the project folder to see the generated bit stream file as shown in the figure below:

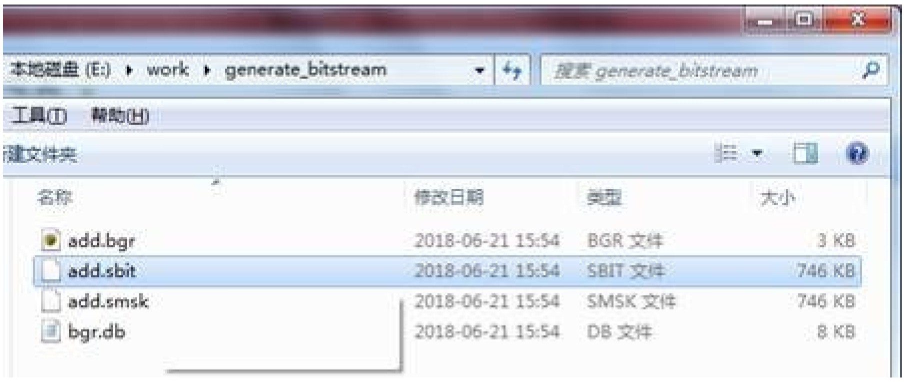


Figure 3-62 generated bitstream files

3.10 Command line operation

Each of the above operations supports direct operations on the command line. You can execute the commands one by one, or write the commands into the tcl script for batch processing. Usage:

source < batch tcl file > ;

After executing it once, you can execute the clean –all command to delete all the previous results, and execute the source command again;

If there is an -option in the command and it runs successfully, it will change the configuration of the project.

For the detailed introduction of command line operation, please refer to the description of command line operation in Chapter 5.

4 Related plugins

When the development process of synthesize , device map , place & route , report timing , report power or generate bitstream is running, it is forbidden to open each plug-in (at this time, the toolbar buttons of each plug-in are unavailable); but the plug-ins that have been opened can still work normally use. Each plug-in can be opened at the same time, but the same plug-in can only be opened once (except the ip configuration interface).

4.1 ADS

For the specific usage of the synthesis tool ADS , please refer to " ADS_Synthesis_User_Guide " and " ADS_Language_Support_Reference_Manual ".

4.2 Synplify_Pro

For the specific usage of the synthesis tool Synplify_Pro , please refer to "fpga_attribute_reference", "fpga_command_reference", "fpga_hdl_reference", "fpga_reference", " fpga_user_guide " in the syn/doc folder under the installation path .

4.3 User Constraint Editor

For specific usage of UCE , please refer to " User_Constraint_Editor_User_Guide ".

4.4 IP Compiler

For specific usage of IP Compiler , please refer to " IP_Compiler_User_Guide ".

4.5 Physical Constraint Editor

For specific usage of PCE , please refer to " Physical_Constraint_Editor_User_Guide ".

4.6 Design Editor

For specific usage of Design Editor , please refer to " Design_Editor_User_Guide ".

4.7 Fabric Inserter

For specific usage of Fabric Inserter , please refer to " Fabric_Inserter_User_Guide ".

4.8 Fabric Debugger

For specific usage of Fabric debugger , please refer to " Fabric_Debugger_User_Guide " .

4.9 Fabric Configuration

For specific usage of Fabric Configuration , please refer to " Fabric_Configuration_User_Guide ".

4.10 Fabric JtagServer

specific usage of Fabric JtagSever , please refer to " Fabric_JtagServer_User_Guide ".

4.11 Pango Power Calculator

For the specific usage of Pango Power Calculator , please refer to "Pango_Power_Calculator_User _Guide ".

4.12 Pango Power Planner

For the specific usage of Pango Power Planner , please refer to "Pango_Power_Planner_User_Guide ".

4.13 Timing Analyzer

For specific usage of Timing Analyzer , please refer to " Timing_Analyzer_User_Guide ".

4.14 Route Constraint Editor

For specific usage of Route Constraint Editor , please refer to " Route_Constraint_Editor_User _Guide ".

4.15 Pango SSN Estimator

Pango SSN Estimator , please refer to " Pango_SSN_Estimator_User_Guide ".

4.16 Pango SSN Analyzer

Pango SSN Analyzer , please refer to " Pango_SSN_Analyzer_User_Guide ".

4.17 Simulation

Simulation , please refer to " Simulation_User_Guide ".

4.18 View RTL Schematic

If the synthesis tool is ADS , the specific usage of View RTL Schematic can be found in " ADS_Synthesis_User_Guide ".

If the synthesis tool is Synplify Pro , for the specific usage of View RTL Schematic , please refer to " fpga_reference " in the syn/doc folder under the installation path .

4.19 View Technology Schematic

If the synthesis tool is ADS , the specific usage of View Technology Schematic can be found in " ADS_Synthesis_User_Guide ".

If the synthesis tool is Synplify Pro , for the specific usage of View Technology Schematic , please refer to " fpga_reference " in the syn/doc folder under the installation path .

5 Command line run

PDS software supports three command line operation modes. We take the pds.exe on Win7 as an example, and introduce them respectively as follows:

5.1 Project operation mode

The -project parameter of pds can run the PDS software by directly opening a project. The operation method is to type in the DOS interface:

C:\Users\pango>C:\pango\PDS_2021.3\bin\pds.exe -project C:\Users\pango\Desktop\project\project.pds

pressing the Enter key, the main interface of the PDS software will open, and the project project.pds has been opened, as shown in the figure below:



Figure 5-1 pds.Exe open pds

5.2 TCL script running mode

Each step in the main process has corresponding commands. These commands can be directly written in a tcl script, and in the Console window of the pds interface as follows , you can source a tcl file to execute.

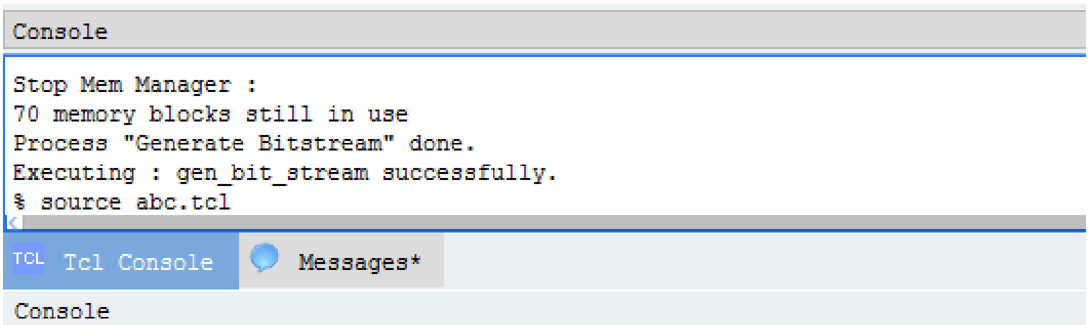


Figure 5-2 Script to run tcl file

A sample script is as follows:

add_design "E:/add.v"

add_design "E:/assign001.v"

set_arch -family Logos -device PGL50H -speedgrade -6 -package FBG484

synthesize -ads -selected_syn_tool_opt 2 -top_module add

dev_map

pnr

report_timing

gen_bit_stream

5.3 Shell operation mode

1. The -file parameter of pds can run the PDS software by directly executing the tcl script file. The operation method is to type in the DOS interface:

```
C:\Users\pango> C:\pango\PDS_2021.3\bin\pds.exe -file F:\work\project\pds\Adder\Adder.tcl –work_dir C:\work_dir –project_name test
```

Among them, work_dir and project_name are optional. Work_dir specifies the working directory, and project_name specifies the project file name. The rules are as follows:

1. When specifying file , if work_dir and project_name are not specified , the project will be stored in the directory at the same level as the tcl file, and the pds project file name will be the same as the tcl file.
2. When specifying file , if you specify work_dir but not project_name , the project is stored in the work_dir option value directory, and the pds project file name is the same as the tcl file.
3. When specifying file , if you do not specify work_dir but specify project_name , the project will be stored in the same directory as the tcl file, and the pds project file name will be the value of the project_name option.
4. When specifying file , if you specify work_dir and project_name , the project is stored in the work_dir option value directory, and the pds project file name is project_name option value.

2. The -project parameter of pds can run the PDS software by opening the .pds project file. The operation method is to type in the DOS interface :

```
C:\Users\pango> C:\pango\PDS_2021.3\bin\pds.exe -project F:\work\project\pds\Adder\project.pds –run gen_bit_stream
```

Among them, run is an optional item, which is used to specify the process step to be run. The rules are as follows:

-run compile Run to Compile

-run synthesize Run to Synthesize

-run dev_map run to Device Map

-run pnr run to Place & Route

-run report_timing run to Report Timing

-run report_power Run to Report Power

-run gen_netlist run to Generate Netlist

-run gen_bit_stream run to Generate Bit Stream

5.4 Commands supported by PDS

Syntax: command [OPTION] ... [OPTION VALUE] ...

example:

add_design "F: /ipcore/rom/inst.idf"

add_constraint -logic -sdc pgdemo.sdc

compile -include_path {C:/Program Files C:/Program Files (x86)}

synthesize –ads

gen_bit_stream -create_bin -startup_sel TCK

Note: In the tcl standard syntax, "\" is an escape character, you may need to change the " \ " in the windows folder path to " / " before running

【 generate_constraint 】 : It is used to export the DB results after pnr in the form of constraints. You can specify the format of the export and the type of constraint resource to be exported, such as:

generate_constraint –file {file_name}

Generate all constraint information in the form of pcf, including IO , group , prim resources .

generate_constraint –file {file_name} –device {APM/PLL/DRM}

Generate constraint information of a specified type of resource in the form of pcf

generate_constraint –file {file_name} –logic

Generate IO and device constraint information in the form of fdc

generate_constraint –file {file_name} –slack -1.0

DB running timing analysis after reading pnr , generating slack value greater than or equal to in txt format

-0.1ns instance location constraint information

generate_constraint –file {file_name} –less_mode –slack -1.0

timing analysis of DB running after reading pnr , the slack value generated in the form of txt is less than

-0.1ns instance location constraint information

generate_constraint –file {file_name} –group

Generate group instance constraint information in the form of fdc

generate_constraint –file {file_name} –prim

Generate constraint information of prim instance in the form of fdc

(Note: The generated constraint files all have the no_check option, that is, the generated IO commands will not perform IO standard checks (that is to say, the settings in the default commands are correct at this time, and the configurations in the commands will work normally on the pnr), the generated instance -related commands will not check whether the instance exists, and the non-existing instance will be ignored)

As in the generated fdc :

define_attribute {clk} {PAP_IO_CHECK_IO} {FALSE}

That is, except for clk 's PAP_IO_LOC , other IO standards will not be checked and passed directly

the generated pcf :

def_port {clk} LOC=A1 IOSTANDARD=LVCMOS33 VCCIO=3.3 CEHCK_IO=FALSE

, except for LOC , other related standards about clk will not be checked, and will be directly passed to pnr

def_inst_site {inst} device_name –no_check

That is, the command will not check the validity of the inst name, if the inst exists, the command will work normally, otherwise the command will be ignored

【 export_fdc 】 : It is used to reverse-convert the pcf result after dev_map into fdc form constraint export, and you can specify the export path and file command

export_fdc –file file_name.fdc

This command can support -no_log , the default is to print the conversion failure prompt information, to close this print information export_fdc –file file_name.fdc –no_log true

6 Timing Constraint Command

6.1 Object get command

The object acquisition command is mainly used to assist the timing constraint and timing report commands. The object in the constraint command and the report command must be acquired through the object acquisition command. The obtained objects come from the design netlist, so the user constraints also use the netlist as the source of constraints. After the design is converted into RTL , the software will display RTL -level graphic display, and the user can directly write the sdc command according to the name of the graphic display.

6.1.1 all_clocks

This command returns all user-defined clocks (generated using create_clock or create_generated_clock). The format is as follows:

all_clocks

6.1.2 all_inputs

Return all input or inout ports that meet the conditions. If no parameters are set, it means returning all input or inout ports in the design .

all_inputs [-level_sensitive | -edge_triggered] [-clock clock_name]

-level_sensitive : Indicates to return the input constrained by set_input_delay and triggered by the level , see set_input_delay .

-edge_triggered : Indicates to return the input constrained by set_input_delay and triggered by the edge , see set_input_delay .

Note: The or symbol is used in the format, which means that only one of the above two parameters can be selected, or neither can be selected. If neither is selected, it means that the trigger mode of the input signal is not considered.

-clock clock_name : This returns all the inputs constrained by set_input_delay and the associated clock name is clock_name , which can be left unselected.

6.1.3 all_outputs

Returns all output or inout ports that meet the conditions. If no parameters are set, it means returning all output or inout ports in the design .

all_outputs [-level_sensitive | -edge_triggered] [-clock clock_name]

-level_sensitive : Indicates to return the output constrained by set_output_delay and triggered by the level , see set_output_delay .

-edge_triggered : Indicates to return the input constrained by set_output_delay and triggered by the edge , see set_output_delay .

Note: The or symbol is used in the format, which means that only one of the above two parameters can be selected, or neither can be selected. If neither is selected, it means that the trigger mode of the output signal is not considered.

-clock clock_name : This returns all the outputs that have been constrained by set_output_delay and the associated clock name is clock_name , which can not be selected.

6.1.4 all_registers

all_registers [-no_hierarchy] [-clock clock_name | -rise_clock clock_name | -fall_clock clock_name] [-cells | -data_pins | -clock_pins | -async_pins | -output_pins] [-level_sensitive | -edge_triggered]

-clock clock_name : Indicates that the clock at the ck input terminal is the register of clock_name.

-rise_clock clock_name : Indicates that the clock at the ck input terminal is clock_name and the trigger edge is a register with a rising edge.

-fall_clock clock_name : Indicates that the clock at the ck input terminal is clock_name and the trigger edge is a register with a falling edge.

Note: Two or symbols are used in the format definition, as follows:

[-clock clock_name | -rise_clock clock_name | -fall_clock clock_name]

Indicates that only one of -clock clock_name , -rise_clock clock_name , and -fall_clock clock_name can be used .

-cells : return instance with register function .

-data_pins : Returns a collection of data pins , the size of which depends on the design itself and other parameters in the command.

-clock_pins : Return a collection of data pins , the size of which depends on the design itself and other parameters in the command.

-async_pins : Return asynchronous set or reset pins .

Note: In the format [-cells | -data_pins | -clock_pins | -async_pins | -output_pins] are separated by an or symbol, which means that only one of these four options can be selected.

-edge_triggered : Indicates edge-triggered registers.

-level_sensitive : Indicates a level-triggered latch.

Note: There is an or symbol in the middle of [-level_sensitive | -edge_triggered] in the format , indicating that only one of these two options can be selected.

-no_hierarchy : Only top-level registers are considered .

6.1.5 get_cells

The design of the cell corresponds to the intance in the netlist , such as and2 , etc. There are many types of design , such as RTL - level netlist, post-synthesis netlist, and netlist after layout and routing . Timing constraints are made on the table, and timing constraints on other netlists are completed internally by the software.

get_cells [-hierarchical] [-hsc separator] [-regexp] [-nocase] [patterns | -of_objects objects]

-hierarchical : Indicates that the net is hierarchical . For example, our design contains multiple modules , and these modules will be instantiated in the top module , then the cells in those instantiated modules are hierarchical , and vice versa. The cell in the module is non- hierarchical .

-hsc separator : hierarchical separator. If the cell is hierarchical , then the name of the module should be added when writing the name, and separated by a separator. For example, if the separator is '_' , there is a cell in module A whose name is unst , and A is instantiated as a , then the name of the cell should be written as a_unst

-regexp : Indicates that regular expressions are supported.

-nocase : Indicates that you don't care about the case of the pattern .

-of_objects objects : Indicates a collection of cells connected to a specific type of objects .

patterns : the name of the instance .

Note: -of_objects objects and patterns can only define one.

6.1.6 get_clocks

clocks that meet the conditions defined by the current user (via create_clock and create_generated_clock) .

get_clocks [-regexp] [-nocase] [-include_generated_clocks] Patterns

-regexp : Indicates that regular expressions are supported.

-nocase : Indicates that you don't care about the case of the pattern .

-include_generated_clocks : The returned clocks include the generated clocks driven by the matched patterns clock .

patterns : the name of the clock .

6.1.7 get_nets

Return all nets in design that satisfy the condition .

get_nets [-hierarchical] [-hsc separator] [-regexp] [patterns | -of_objects objects]

-hierarchical : Indicates that the net is hierarchical . For example, our design contains multiple modules , and these modules will be instantiated in the top module , then the nets in those instantiated modules are hierarchical , and vice versa . The net in the module is non- hierarchical .

-hsc separator : hierarchical separator. If the net is hierarchical , then the name of the module should be added when writing the name, and separated by a separator. For example, if the separator is '_' , there is a net name in module A that is reset , then the name of the net should be written for A_reset .

-regexp : Indicates that regular expressions are supported.

-nocase : Indicates that you don't care about the case of the pattern .

-of_objects objects : Indicates the net collection connected to a certain type of specific objects . The object can be a cell (instance), which returns all the nets on the cell (instance). The object can also be a pin , and returns all the nets connected to the pin net , or port , returns the net connected to this port .

patterns : the name of the net .

Note: -of_objects objects and patterns can only define one.

6.1.8 get_pins

Return all pins in the design that meet the conditions .

get_pins [-hierarchical] [-hsc separator] [-regexp] [-nocase] [patterns | -of_objects objects]

-hierarchical : Indicates that the pin is hierarchical . For example, our design contains multiple modules , and these modules will be instantiated in the top module , then the pins in those instantiated modules are hierarchical , and vice versa. The pins in the module are non- hierarchical .

-hsc separator : hierarchical separator. If the pin is hierarchical , then the name of the module should be added when writing the name, and separated by a separator. For example, if the separator is '_' , there is a pin in module A whose name is reset , then the name of the pin should be written for A_reset

-regexp : Indicates that regular expressions are supported.

-nocase : Indicates that you don't care about the case of the pattern .

-of_objects objects : Indicates the collection of pins connected to a certain type of objects . The object can be a cell (instance), which returns all the pins on the cell (instance). The object can also be a net , and returns all the pins connected to the net . pin , can also be a port , return the pin connected with this port .

patterns : The name of the pin .

Note: -of_objects objects and patterns can only define one.

6.1.9 get_ports

Returns all ports in the design that satisfy the condition .

get_ports [-regexp] [-nocase] [patterns]

-regexp : Indicates that regular expressions are supported.

-nocase : Indicates that you don't care about the case of the pattern .

patterns : the name of the port .

Note: -of_objects objects and patterns can only define one.

6.2 Clock Constraint Command

6.2.1 create_clock

The command format is as follows:

create_clock

-period <period_value>

[-name <clock_name>]

[-waveform <edge_list>]

[-add]

[<source_objects>]

[-disable]

The meaning of each parameter in the command is explained as follows, the square brackets indicate that the parameter is an optional value, and the angle brackets indicate the parameter value or parameter list:

-period : Define the period of creating the clock, which is a floating point number and the unit is ns .

[-name] : The name of the created clock, if it is not defined, you must specify source_objects , and the name is the same as the name of the first parameter in source_objects ; if the user does not define source objects , the user must define -name , at this time The created clcok is a virtual clock.

[-waveform] : Define the positions of the rising and falling edges of the clock, where the rising edge is in front and the falling edge is in the rear, and exist in pairs. The format is as follows:

-waveform {time_rise time_fall time_rise time_fall ...}

[-add] : Indicates that multiple clocks can be defined on the same pin. If a clock has been defined on the source_object before , and the user has not added the -add parameter, that is, the user has not specified how many clocks need to be defined on the pin or port . clock, then the clock defined later will overwrite the previous one, and the software will give a warning.

[<source_objects>] : The source of the created clock, which can be pin or port (note that it must be obtained through get_pins and get_ports).

[-disable] : Make this constraint ineffective.

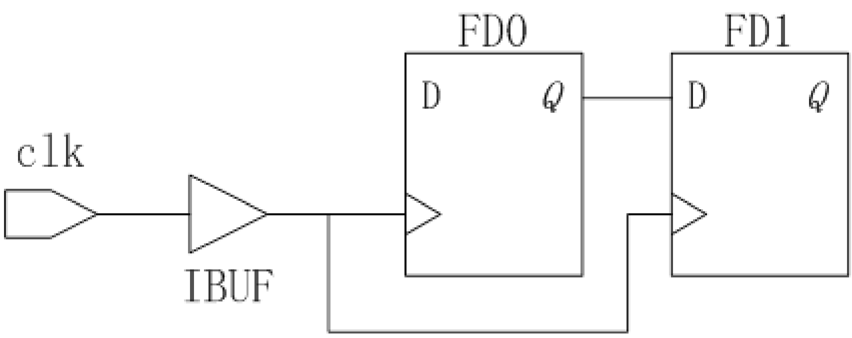


Figure 6-1 clock creation instance

clk signal controls the launch and capture time of the FD0 and FD1 flip-flops. In order to ensure that the timing path setup and hold time checks from the FD0/C terminal to the FD0 /D terminal are accurate, a clock needs to be created at the input port clk , for example:

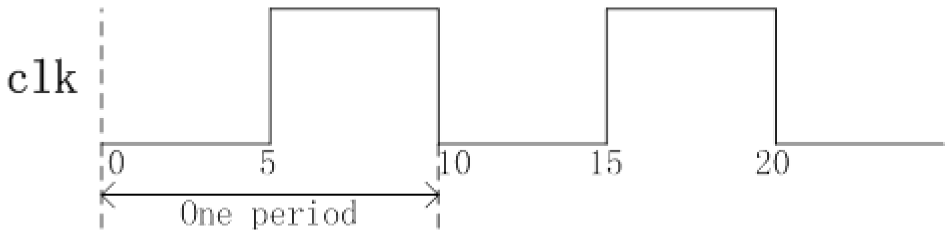


Figure 6-2 clocks to create a waveform diagram

constraint command is as follows: create_clock -name clk -period 10 -waveform {5 10} [get_ports clk]

6.2.2 create_generated_clock

create_generated_clock

[-name <clock_name>]

-source <master_pin>

[-master_clock <clock>]

[-edges <edge_list>] [-edge_shift <shift_list>]

[-multiply_by <factor>] [-divide_by <factor>]

[-duty_cycle <percent>]

[-invert]

[-add]

<source_objects>

[-disable]

The meaning of each parameter in the command is explained as follows, the square brackets indicate that the parameter is an optional value, and the angle brackets indicate the parameter value or parameter list:

[-name] : The name of the clock to create.

-source : Specify the pin or port of the source clock to drive the generated clock .

[-master_clock] : Specify the source clock . There are multiple source clocks on the master pin , and the generated clock only comes from one of the clocks . When there is only one source clock on the master pin , this parameter can not be specified.

[-edges] : Indicates the list of edges referenced from the source clock . Each edge cannot be less than 1 and cannot be less than the previous edge , which is consistent with the waveform format in create_clock ; the difference is that the second cycle starts at the end. Position, PDS requires that the number of parameters in the edge_list must be 3 , which not only includes the rising edge and falling edge of the first cycle, but also the rising edge of the second cycle, from which the software can calculate the cycle of the generated clock ; As shown below:

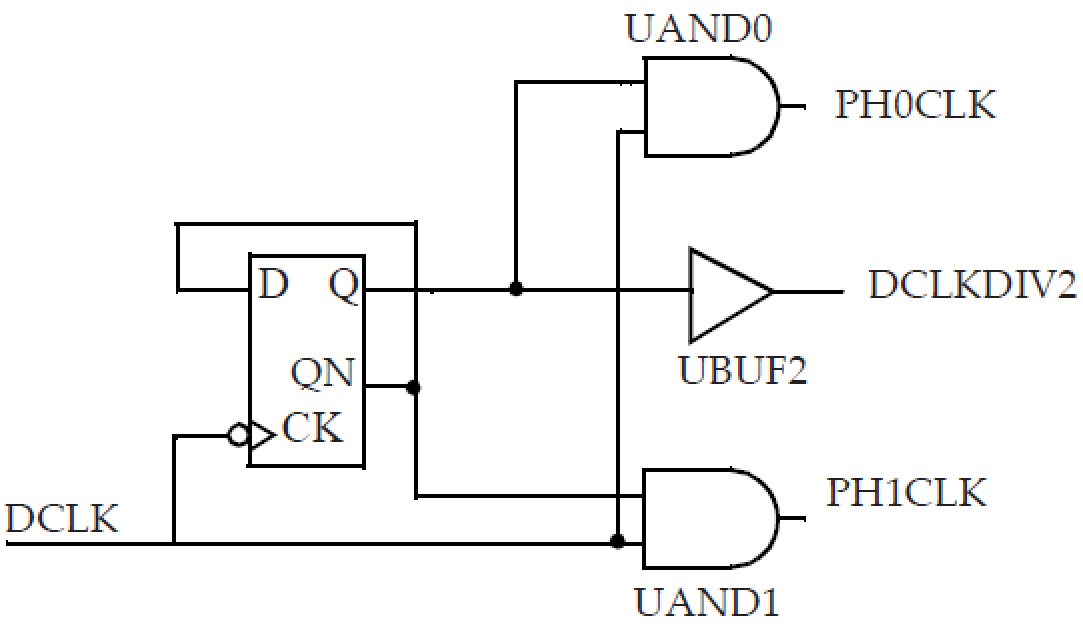


Figure 6-3 generated clock period calculation

For DCLKDIV2 , its waveform is as follows:

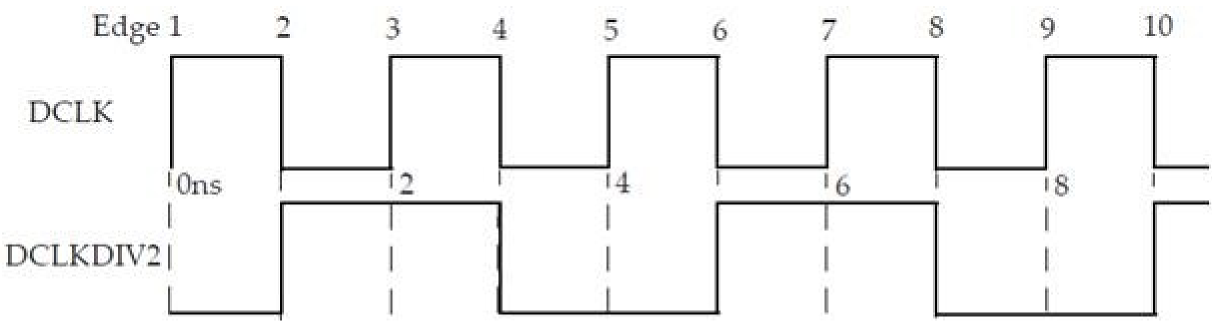


Figure 6-4 DCLKDIV2 waveform

The corresponding constraints are as follows:

create_generated_clock -name DCLKDIV2 -edges {2 4 6} -source DCLK [get_pins UBUF2/Z]

Among them, 2 represents the second edge of the source clock , "4" represents the fourth edge of the source ... and so on; in the generated clock , "2" corresponds to the first rising edge position, and "4" represents the first falling edge Edge position, "6" indicates the position of the next rising edge.

[-edge_shift] : Specify a series of floating point numbers to represent the offset of each edge, the unit is ns , and must be used together with -edges ; if the generated clock needs to implement the phase shift function, then you need to use "-edge_shift " , the number of list elements in "-edge_shift" must be the same as the number in "-edges" .

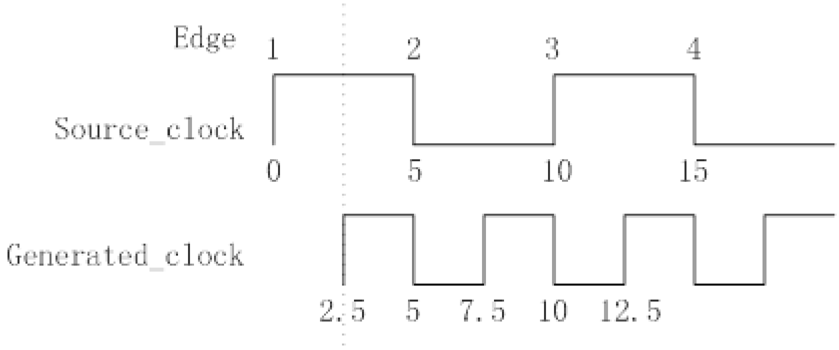


Figure 6-5 Phase shift waveform example

Example in the above figure, the generated clock implements the function of frequency multiplication and 90 -degree phase shift for the source clock , which can be written in the following format:

create_generated_clock -name generated_clock -source master_pin

-edges {1 2 3} -edge_shift {2.5 0 -2.5} [get_pins PLL/OUT0]

In this command, it can be seen from the -edges parameter that the first rising edge, the first lower edge, and the second rising edge of the generated clock correspond to edge1 , edge2 , and edge3 of the source clock respectively, and from the -edge_shift parameter, the generated clock 's The first rising edge is offset to the right by 2.5 time units relative to edge1 of the source clock , the first falling edge is not offset compared to edge2 of the source clock , and the second rising edge is offset to the left relative to edge3 of the source clock Shifted by 2.5 is the time unit.

[-multiply_by] : Frequency multiplication coefficient. The frequency multiplication coefficient is an integer greater than 0 , which reduces the clock cycle by a specified multiple . Frequency multiplication not only causes changes in the cycle, but also reduces the waveform proportionally.

[-divide_by] : Frequency division coefficient, the frequency division coefficient is an integer greater than 0 , which expands the clock cycle by a specified multiple. Frequency division not only causes changes in the period, but also changes in the waveform. In PDS , when the frequency division coefficient is 2 and the exponential multiple of 2, the duty cycle will be set to 50 % , and the other coefficient values will keep the original duty cycle unchanged.

-divide_by and -multiply_by can be used at the same time, either -divide_by or -multiply_by can be used first; frequency division and multiplication can be used at the same time to achieve frequency conversion of non-integer multiples, that is, decimal frequency division, which can be set in the UCE interface multiply_devide_by to achieve fractional frequency division, as follows:

create_generated_clock -name MIIDIV2 -source MICK –mutiply_by 2 –devide_by 3 [get_pins UMIIDIV/Q]

[-duty_cycle] : The unit is percent (%), which describes the duty cycle, that is, the proportion of the high level to the entire cycle. The duty cycle can only be used when using -multiply_by ;

[-invert] : Indicates that the clock signal of the generated clock is inverted relative to the source clock . As shown below:

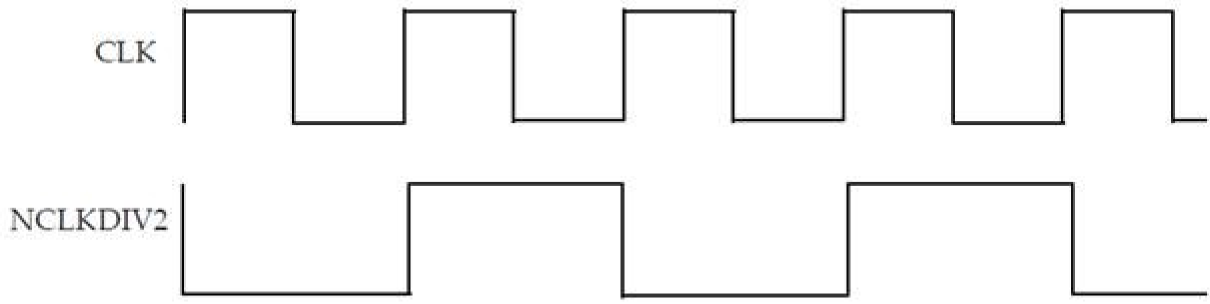


Figure 6-6 Invert instance

The corresponding constraint commands are as follows:

create_generated_clock -name NCLKDIV2 -divide_by 2 -invert -source CLK [get_pins UINVQ/Z]

[-add] : If a clock of the same type has been defined for this pin before , then adding the -add option will add a new clock on the basis of the previous one , if the user does not add this option, then the newly created clock will be The original clock will be replaced. If multiple clocks of the same type are defined on the same source object , these multiple clocks are physically independent.

<source_objects> : the pin , port or net of the generated clock to be created .

[-disable] : Make this constraint ineffective.

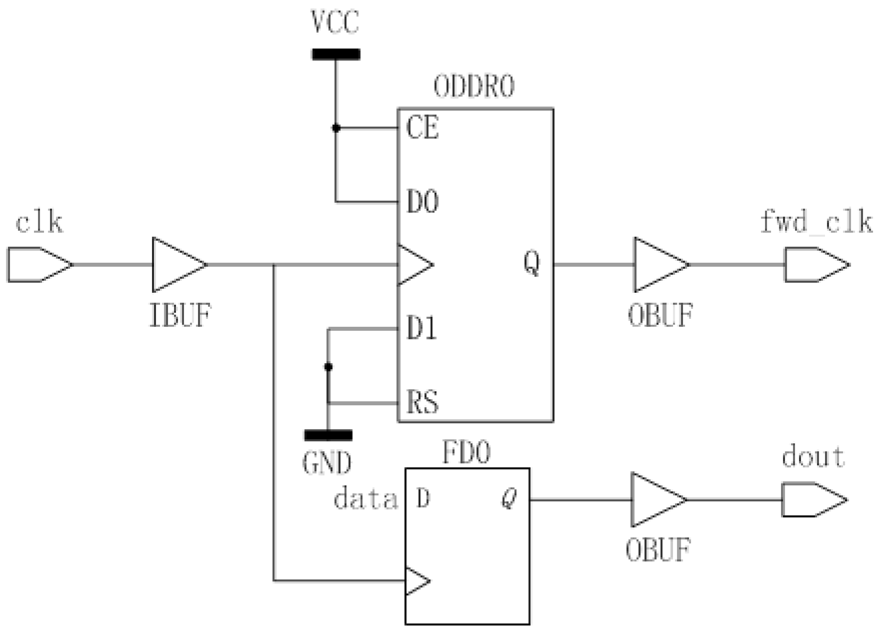


Figure 6-7 example of the channel-associated clock

clock is defined at the output port and replicates the generated clock of the internal clock signal of the FPGA . The associated clock is usually used as the reference clock of other output ports under the source clock synchronization interface. When setting the output delay of the output port , it can be assigned to the associated clock to check whether the timing requirements of the source synchronous interface are met. Create an accompanying clock as shown in the figure, and the constraints are as follows:

create_generated_clock -name fwd_clk -divide_by 1 -source [get_pins ODDR0/C] [get_ports fwd_clk]

Note:

1. -edges/-edge_shift cannot be used together with -multiply_by , -divide_by , -duty_cycle .

2. For the create_generated_clock constraint created by the user on the PLL , if the PLL is configured with a phase shift, then the constraint command needs to use the -edges/-edge_shift option to reflect the phase shift information of the PLL on the waveform of the generated clock ; the software automatically displays it on the PLL The infer clock also reflects the phase shift delay of the PLL through the above method. In addition, users need to pay attention to the clock edge pairs

on the timing analysis path, which may sometimes need to be adjusted through the set_multicycle_path constraint.

3. The create_generated_clock command supports the rename function, that is, the user only needs to specify -name and source_objects in create_generated_clock , and the software will automatically infer the cycle and waveform of the clock. You can also specify -source | -master_clock to filter the source clock. This function only Clock output port that supports PLL and CLKDIV . If the user wants to use this feature, the following options cannot be specified: [-edges edge_list] [-edge_shift shift_list] [-divide_by factor] [-multiply_by factor] [-duty_cycle percent] [-invert] . Users can use this function to rename the generated clock of the software infer , and perform subsequent timing constraints based on the specified name. The Rename clock can no longer be used as the source clock of the generated clock clock. An example command is as follows:

create_generated_clock -name pll_clk [get_pins {pll.clkout1}]

6.2.3 set_clock_latency

set_clock_latency only supports source latency , not network latency , and the -source parameter must be defined in the constraint . Source latency is mainly used to define the delay information between the clock generation point and the clock definition point. That is, as shown in the figure below:

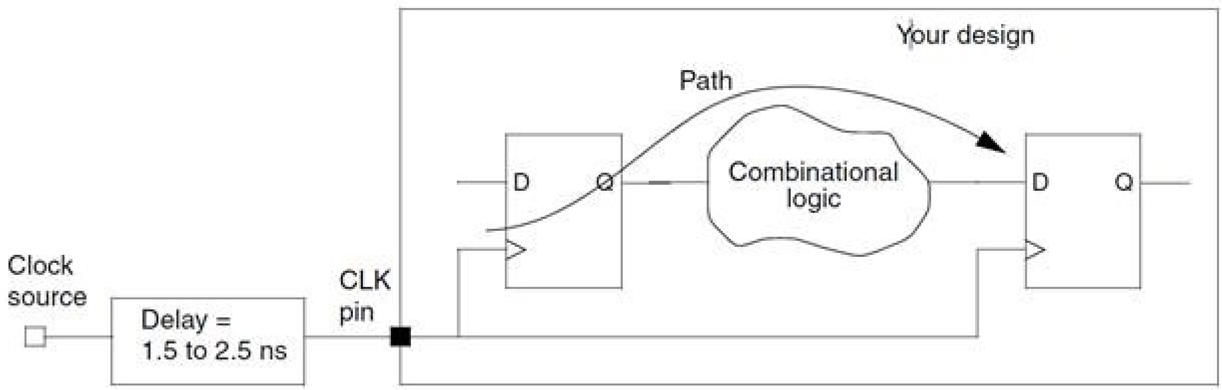


Figure 6-8 Schematic diagram of Source latency

Among them, CLK pin is the definition point of the FPGA input clock, Clock source is the generation point of the clock, and source latency is the delay information between these two points. The specific commands and parameters are introduced as follows:

set_clock_latency

[-clock <clock_list>]

[-rise] [-fall]

[-min] [-max]

[-early] [-late]

– source

<object_list>

<latency_value>

[-disable]

The meaning of each parameter in the command is explained as follows, the square brackets indicate that the parameter is an optional value, and the angle brackets indicate the parameter value or parameter list:

[-clock] : When multiple clocks are defined on the pin/port of the object_list , this option is used to filter the clocks specified by the user. When using it, it needs to follow the principle of declaration before use, that is: clock needs to be created by create_generated_clock or create_clock first .

[-rise] : Indicates that the latency is only applied when the trigger clock edge is a rising edge.

[-fall] : Indicates that the latency is only applied when the trigger clock edge is a falling edge.

[-min] : If it is used in bc_wc environment, -min means fast corner , -max means slow corner ; if -min and -max are not specified , the default fast corner and slow corner commands will take effect, but -min and -max cannot specified at the same time. -early indicates that the latency is the left offset of the clock , -late indicates that the latency is the right offset of the clock ; if -early and -late are not specified , the left and right offsets of the default clock will take effect, but -early and -late Cannot be specified at the same time.

[-max] : See the explanation of min .

[-early] : See the explanation of min .

[-late] : See the explanation of min .

-source : Indicates that the latency is source latency , which must be specified in the constraint.

object_list : clock definition point , which is the clock definition point. The clock defined on the corresponding pinport can be obtained through get_pins and get_ports , or the latency can be directly defined on the clock .

<latency_value> : Latency value, which is a floating point number, and the unit is ns .

[-disable] : Make this constraint ineffective.

An example command is as follows:

#The rising edge source latency clock delay on MAIN_CLK is 1.8ns:

set_clock_latency 1.8 -rise [get_clocks MAIN_CLK] –source

#The falling edge source latency clock delay on all clocks is 2.1ns

set_clock_latency 2.1 -fall [all_clocks] –source

6.2.4 set_clock_uncertainty

The role of set_clock_uncertainty is explained at set_clock_latency .

set_clock_uncertainty

[<uncertainty_value>]

[-setup] [-hold]

[<object_list> |

-from <from_clock>

| -rise_from <rise_from_clock>

| -fall_from <fall_from_clock>

-to <to_clock>

| -rise_to <rise_to_clock>

| -fall_to <fall_to_clock>]

[-disable]

The meaning of each parameter in the command is explained as follows. The square brackets indicate that the parameter is an optional value, the angle brackets indicate the parameter value or parameter list, and the | indicates the or symbol. Multiple options at the same level can only use one:

[-from] : Indicates the launch clock , regardless of the polarity of the clock. When using the clock , you need to follow the principle of declaration before use, that is, the clock needs to be created by create_generated_clock or create_clock first .

-rise_from : Indicates that only the rising edge of the launch clock is considered. When using the clock , you need to follow the principle of declaration before use, that is, the clock needs to be created by create_generated_clock or create_clock first .

-fall_from : Indicates that only the falling edge of the launch clock is considered. When using the clock , you need to follow the principle of declaration before use, that is, the clock needs to be created by create_generated_clock or create_clock first .

[-to] : Indicates the capture clock , regardless of the polarity of the clock. When using the clock , you need to follow the principle of declaration before use, that is, the clock needs to be created by create_generated_clock or create_clock first .

-rise_to : Indicates that only the rising edge of the capture clock is considered. When using the clock , you need to follow the principle of declaration before use, that is, the clock needs to be created by create_generated_clock or create_clock first .

-fall_to : Indicates that only the falling edge of the capture clock is considered. When using the clock , you need to follow the principle of declaration before use, that is, the clock needs to be created by create_generated_clock or create_clock first .

-setup : Indicates that the uncertainty value is only used in setup analysis.

-hold : Indicates that the uncertainty value is only used in hold analysis.

uncertainty : The value of uncertainty , which is a floating point number, and the unit is ns .

object_list : If multiple clocks are defined on the pin or port of the clock end of the trigger , and the user only wants to define uncertainty for one of the clocks , then object can be a clock defined by the user. If the user wants to set the pin on the terminal for the trigger All clocks define the same uncertainty , and that object can be a pin or port . Note: All objects must be obtained through the three commands get_clocks , get_pins , and get_ports . When using get_clock , you need to follow the principle of declaration before use, that is, the clock needs to be created through create_generated_clock or create_clock first .

[-disable] : Make this constraint ineffective.

Note: There is an or symbol between [object_list] , [-from from_clock | -rise_from rise_from_clock | -fall_from fall_from_clock] and [-to to_clock | -rise_to rise_to_clock | Choose one of two formats, either object_list or -from -to.

The clock period jitter and the extra margin in the timing check can be set with set_clock uncertainty , specifying setup and hold to change the effective clock period, as shown in the following figure:

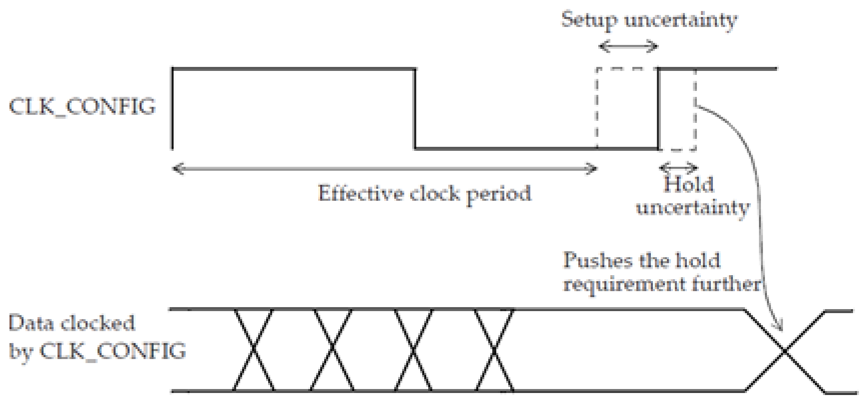


Figure 6-9 Schematic diagram of set_clock uncertainty

The command is as follows:

set_clock_uncertainty -setup 0.2 [get_clocks CLK_CONFIG]

set_clock_uncertainty -hold 0.05 [get_clocks CLK_CONFIG]

Note: The PDS software will add a certain jitter to the constrained clock by default through the command set_clock_uncertainty , such as 50ps system jitter and 150ps pll jitter .

6.2.5 set_clock_group

When using this command, the clock in the option group needs to follow the principle of declaration before use, that is: the clock needs to be created by create_generated_clock or create_clock first , and then it can be used in set_clock_groups . The command format is as follows:

set_clock_groups

[-name group_name]

[-asynchronous | -logically_exclusive | -physically_exclusive]

-group <clock_list>*

[-disable]

The meaning of each parameter in the command is explained as follows. The square brackets indicate that the parameter is an optional value, the angle brackets indicate the parameter value or parameter list, * indicates that the parameter can be repeated, | indicates the or symbol, and multiple options at the same level can only use one :

[-name] : The name of the clock group .

[-logically_exclusive] : Indicates that each clock in the clock group is logically independent. The so-called logical independence means that there are clock paths between physically different clocks and clock pins , but logically the paths will not be opened at the same time, a typical example is mux , examples are as follows:

Example 1 : Logically exclusive with no interaction

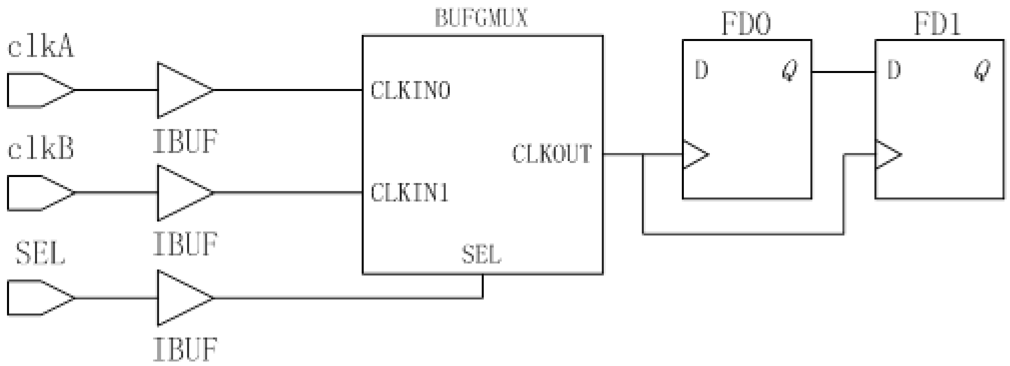


Figure 6-10 Logically exclusive with no interaction Example

In this example, there is no logic path between clkA and clkB , nor is it shared by any combinational logic unit driven by BUFGMUX . Therefore, we can directly set the exclusive clock group between clkA and clkB , so that no real timing path is missed from analysis. The constraint command is: set_clock_groups -logically_exclusive -group clkA -group clkB

Example 2 : Logically exclusive with interaction

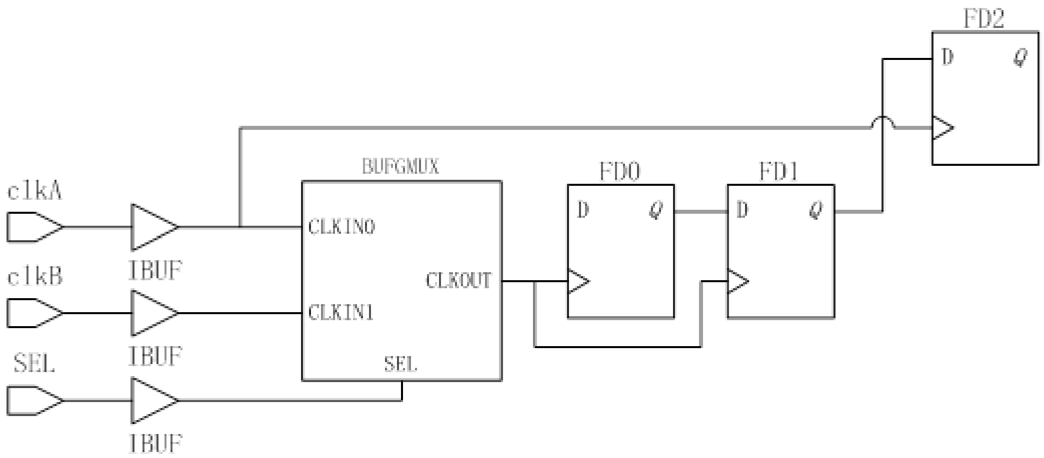


Figure 6-11 Logically exclusive with interaction example

In this example, clkA and clkB are input to a BUFGMUX whose output clock drives two flip-flops FD0 and FD1 . At the same time , clkA also drives the flip-flop FD2 of the timing path between FD1 and FD1 . So there is an influence between clkA and the output clock of BUFGMUX . In this case, it is not recommended to directly set the clock group between clkA and clkB , because this setting will ignore the timing analysis between FD1 and FD2 when BUFGMUX selects clkB . Therefore, you can first set two generated clocks for the output clock of BUFGMUX , and then set the clock group for these two generated clocks.

The constraint commands are as follows:

create_generated_clock -name clkAmux -divide_by 1 \

-source [get_pins BUFGMUX/I0] [get_pins BUFGMUX/O]

create_generated_clock -name clkBmux -divide_by 1 \

-source [get_pins BUFGMUX/I1] [get_pins BUFGMUX/O]\

-add -master_clock clkB

set_clock_groups -logically_exclusive -group clkAmux -group clkBmux

-physically_exclusive : Indicates that each clock in the clock group is physically independent. The so-called physical independence means that there is no real connection between each clock . It is just a different situation under different analysis conditions, typically in the same clock pin Multiple clocks are defined above. In practice, it is obviously impossible for these clocks to exist at the same time. Examples are as follows:

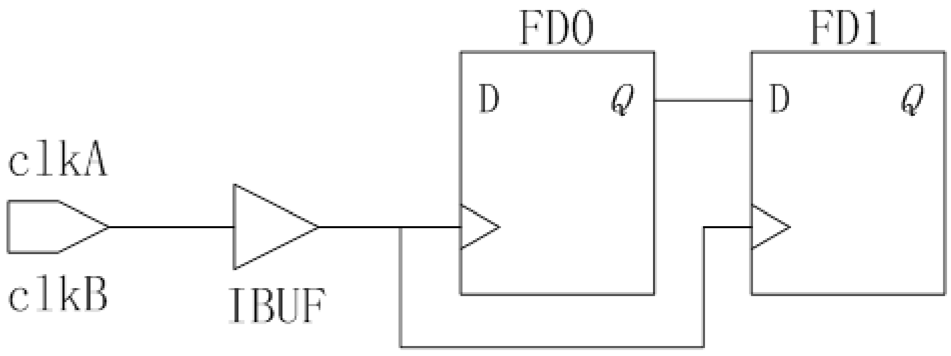


Figure 6-12 Physically exclusive Example

In this example, two main clocks clkA and clkB are defined on the same input port clk .

create_clock -period 10.000 -name clk_A -waveform {0.000 5.000} \

[get_ports clk]

create_clock -period 20.000 -name clk_B -waveform {0.000 10.000} \

-add [get_ports clk]

Because clkA and clkB cannot take effect at the same time, it is necessary to set a physically exclusive group to prevent analysis between these two clocks.

set_clock_groups -physically_exclusive -group clkA -group clkB

For the clock fanout that may be caused by the design logic, you can use -include_generated_clock to include the main clock and its generated clock when setting constraints.

set_clock_groups -physically_exclusive \

-group [get_clocks -include_generated_clock clkA] \

-group [get_clocks -include_generated_clock clkB]

-asynchronous : Indicates that each clock between clock groups is asynchronous. The software will not analyze asynchronous circuits, examples are as follows:

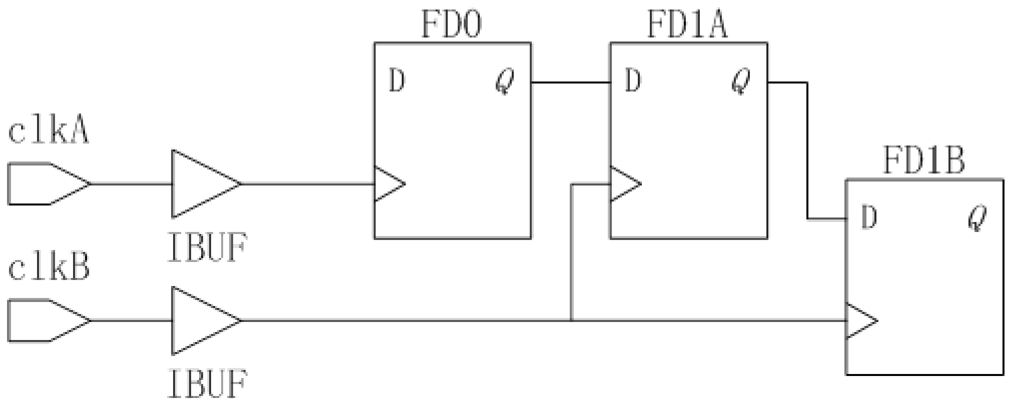


Figure 6-13 Asynchronous example

In this example, clk0 and clk1 are input to the device from different ports , and the phase relationship between them cannot be known. Hence they are asynchronous. By default, the path from FD0 to FD1A is considered a regular synchronous path by timing analysis tools unless a timing exception is added.

Because clk0 and clk1 are asynchronous, the setup and hold time margins at the D side of the FD1A flip -flop cannot be accurately calculated , which means that the FD1A flip-flop may be in a metastable state. In the above example, FD1A and FD1B form a dual-register synchronizer, which can significantly reduce the probability of metastable state propagation.

In this example, there is only one path from clk0 to clk1 but no path from clk1 to clk0 , so the following two constraints have the same effect.

set_clock_groups -asynchronous -group clk0 -group clk1

set_false_path -from [get_clocks clk0] -to [get_clocks clk1]

Note: The three options -logically_exclusive -physically_exclusive -asynchronous are equivalent in the timing analysis process, and all represent the asynchronous relationship between clocks.

-group clock_list : Note that the format of this parameter is followed by a "*" , "*" indicates that the parameter can be repeated, that is, the command can specify multiple groups , and the two clocks between different groups are asynchronous; each group One or more clocks can be specified , and the clocks in the same group are in a synchronous relationship, that is, timing analysis will be performed; when only one group is specified , then the clocks in this group are in a synchronous relationship, and are not included in this The other clocks in the group are all asynchronous, and

this asynchronous relationship also includes the generated clock derived from them . Examples are as follows:

Example 1 : set_clock_groups –name grp0 -asynchronous -group [get_clocks {CLK}] , indicating that the clock CLK and other clocks (including its derived clocks) are asynchronous. If you need to perform timing analysis between the clock CLK and its derived clock, you need to write the derived clock through the create_generated_clock constraint, and then constrain them to the same group , as follows: set_clock_groups –name grp0 -asynchronous -group {CLK CLK_DRV} .

Example 2 : set_clock_groups - logically_exclusive -name grp1 -group {CLK33} -group {CLK50} , which means and only means that the clock CLK33 and the clock CLK50 are asynchronous.

Example 3 : set_clock_groups - physically_exclusive -group {CLK1 CLK3} -group {CLK2 CLK4} , which means that the clocks CLK1 and CLK3 in the same group are in a synchronous relationship, and CLK2 and CLK4 are also in a synchronous relationship, and timing analysis will be performed, but between the two groups The pairwise clocks are asynchronous.

Example 4 : set_clock_groups –name grp0 -asynchronous -group [get_clocks {CLK} –include_generated_clocks] , indicating that the clock CLK and the generated clock derived from it are synchronous, and are asynchronous with other clocks.

6.3 IO Timing Constraint Command

6.3.1 set_input_delay

set_input_delay command specifies the delay of the input path on the input port at the design interface relative to a certain clock edge. The command format is as follows:

set_input_delay command specifies the delay of the input path on the input port at the design interface relative to a certain clock edge. The command format is as follows:

set_input_delay

-clock <clock_name>

[-clock_fall]

[-rise] [-fall]

[-max] [-min]

[-add_delay]

[-source_latency_included]

<delay_value>

<port_list>

[-disable]

-clock : Indicates the name of its associated capture clock. When using clock , you need to follow the principle of declaration before use, that is: clock needs to be created by create_generated_clock or create_clock first .

[-clock_fall] : Indicates that only the falling edge of the trigger clock is considered.

[-rise] : That is, only consider the case where the input signal at the input is a rising edge.

[-fall] : Only consider the case where the input signal at the input is a falling edge.

Note: If the user does not define both, then the software will consider the rise or fall of the input signal at the input at the same time.

[-max] : Indicates that the user-defined delay value is the maximum value.

[-min] : Indicates that the user-defined delay value is the minimum value.

Note: If neither is defined by the user, the software will use the user-defined delay value in both the maximum and minimum delay analysis.

[-add_delay] : If the user has set_input_delay constraints on the input port before , then adding this option means that the software will retain the previously set constraint values. For the case of -max , the delay value will use the same value when calculating The case is calculated by the maximum value of all values, and for the case of -min , the calculation will be performed by the minimum value of all values in the same case.

[-source_latency_included] : Indicates that the delay value (the delay of the data path) has been subtracted from the clock source delay of the timing path. In this case, relative to the delay value, the delay value of the clock path source is 0 . If this option is not included, the source latency of the clock path needs to be specified in front of set_clock_latency . If not specified, then defaults to 0 .

<delay_value> : delay value, which is a floating point number.

<port_list> : input port , the user must get it through get_ports .

[-disable] : Make this constraint ineffective.

Note: The calculation method of the delay value parameter of the set_input_delay command is related to the synchronization method of the input data. Next, the calculation under the system synchronization and source synchronization interfaces will be introduced respectively.

System Synchronous Interface (System Synchronous Interface): Both the sending end and the receiving end are driven by a common system clock, which is called system synchronous input (system synchronous input). The clock signal of the system synchronous interface is completely synchronized by the system board level, and the data transmission delay It cannot be determined at this time and is not suitable for high-speed data transmission.

Under the system synchronous interface, only the edge-aligned mode (clock and data change at the same time), according to the data speed and capture edge is divided into three types: rising edge, falling edge and double edge:

The edge-aligned mode is the most basic input delay mode. The clock captures data in the next cycle. It is necessary to consider the delay of the board trace and the connection line at the same time. In this case, use the edge-aligned mode to constrain the calculation formula.

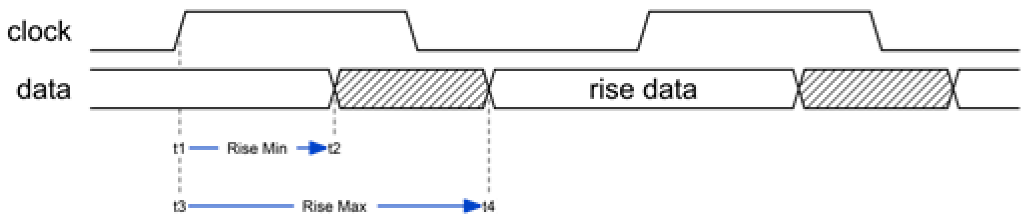


Figure 6-14 System Edge Rise Waveform Diagram

Rise Min = tco_min + trce_dly_min

Rise Max = tco_max + trce_dly_max

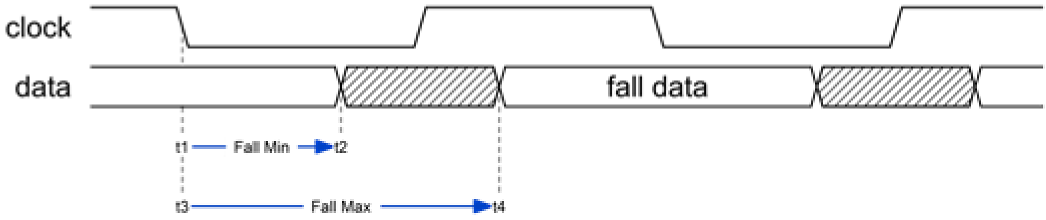


Figure 6-15 System Edge Fall waveform

Fall Min = tco_min + trce_dly_min

Fall Max = tco_max + trce_dly_max

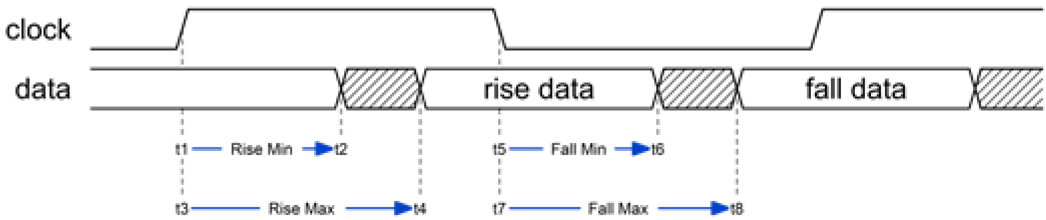


Figure 6-16 System Edge Dual Waveform Diagram

Rise Min = trco_min + trce_dly_min

Rise Max = trco_max + trce_dly_max

Fall Min = tfco_min + trce_dly_min

Fall Max = tfco_max + trce_dly_max

Source Synchronous Interface (Source Synchronous Interface): When the sender sends data, it sends a clock signal of the same source as the input data at the same time. The input data and clock maintain a definite phase relationship, which can support high-speed data transmission.

Under the source synchronous interface, there are center-aligned mode (clock flips at the center of the data valid window), direct edge-aligned mode (clock flips at the beginning of the data valid window) and PLL phase-advance edge-aligned mode (clock flips at the end of the data), according to the data speed and capture edge, it is divided into three types: rising edge, falling edge and double edge:

The center-aligned mode is the most commonly used source synchronous mode. The usage scenario is that the clock is changed in the data center. At this time, the center-aligned mode is used to constrain the calculation formula.

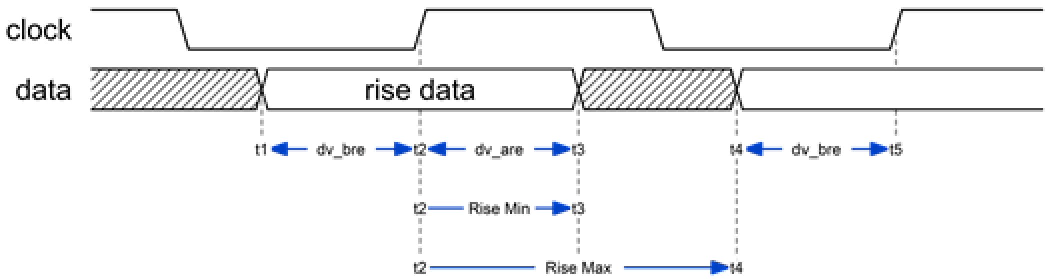


Figure 6 -17 Source Center Rise waveform

Rise Min = dv_are

Rise Max = period - dv_bre

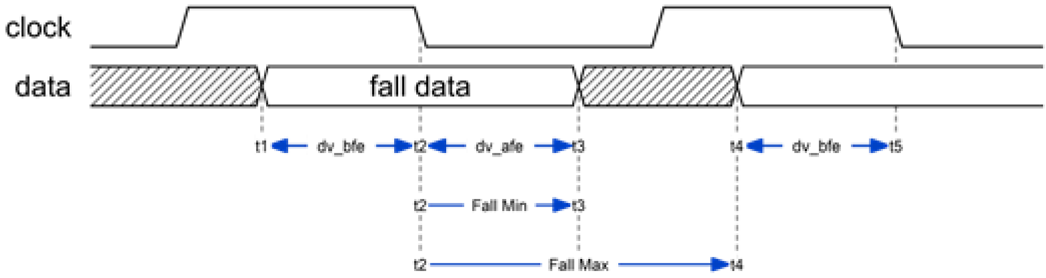


Figure 6 -18 Source Center Fall Waveform Diagram

Fall Min = dv_afe

Fall Max = period - dv_bfe

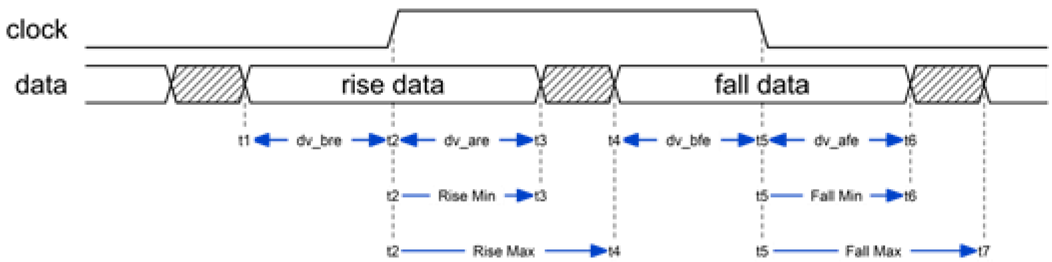


Figure 6-19 Source Center Dual Waveform Diagram

Rise Min = dv_are

Rise Max = (period/2) - dv_bfe

Fall Min = dv_afe

Fall Max = (period/2) - dv_bre

The direct edge alignment mode uses scenarios for clock and data edge alignment. In this case, in order to ensure that the data is accurately captured, it is necessary to use IODELAY to delay the clock and data according to the situation to achieve a center-aligned effect. In this case, use the direct edge alignment mode to constrain the calculation formula.

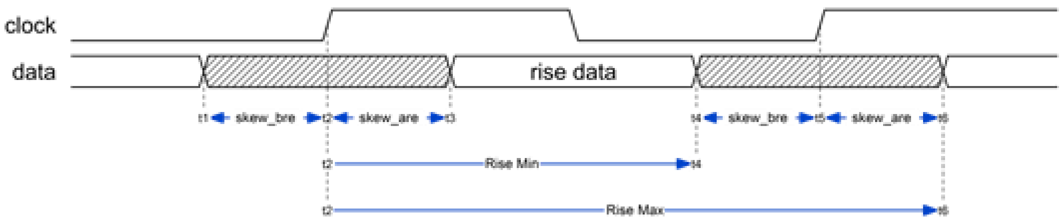


Figure 6-20 Source Edge Direct Rise waveform

Rise Min = period - skew_bre

Rise Max = period + skew_are

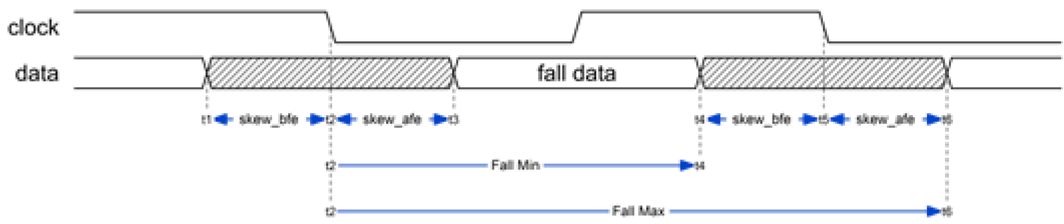


Figure 6-21 Source Edge Direct Fall waveform

Rise Min = period - skew_bfe

Rise Max = period + skew_afe

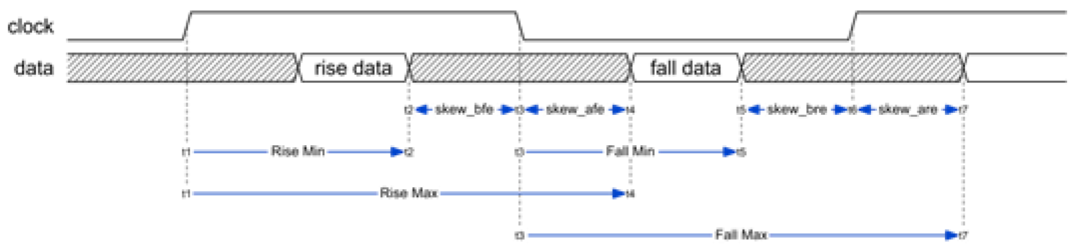


Figure 6 -22 Source Edge Direct Dual waveform

Rise Min = (period/2) - skew_bfe

Rise Max = (period/2) + skew_afe

Fall Min = (period/2) - skew_bre

Fall Max = (period/2) + skew_are

PLL phase advance edge alignment mode is similar to the direct edge alignment usage scenario. The PLL is used to advance the clock phase to capture data correctly. In this case, the PLL phase advance edge alignment mode is used to constrain the calculation formula.

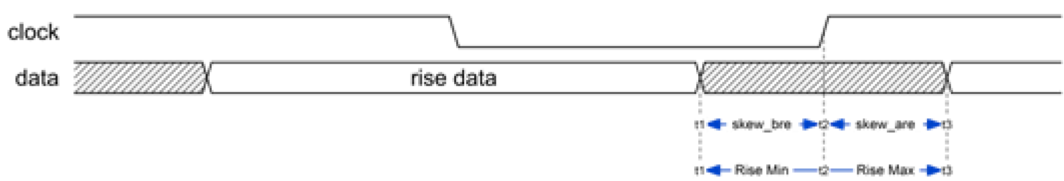


Figure 6 -23 Source Edge PLL Rise waveform

Rise Min = - skew_bre

Rise Max = skew_are

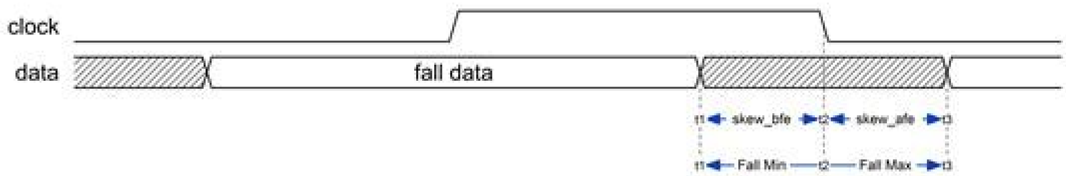


Figure 6-24 Source Edge PLL Fall waveform

Fall Min = - skew_bfe

Fall Max = skew_afe

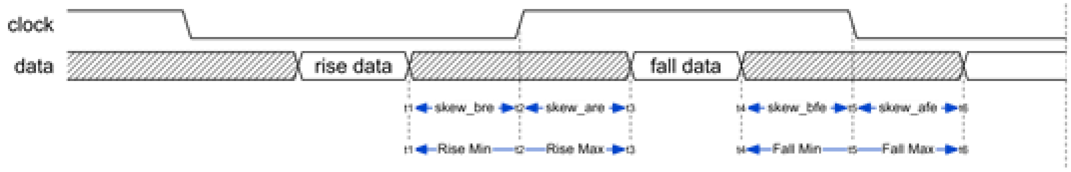


Figure 6 -25 Source Edge PLL Dual waveform

Rise Min = - skew_bre

Rise Max = skew_are

Fall Min = - skew_bfe

Fall Max = skew_afe

The detailed meanings of the abbreviations in the calculation expressions are as follows:

tco_min : Minimum clock to ouput delay (external device) external device minimum clock to output port delay

trco_min : Minimum clock to ouput delay from rising edge (external device) rising edge external device minimum clock to output port delay

tfco_min : Minimum clock to ouput delay from falling edge (external device) external device minimum clock to output port delay on the falling edge

tco_max : Maximum clock to ouput delay (external device) external device maximum clock to output port delay

trco_max : Maximum clock to ouput delay from rising edge (external device) rising edge external device maximum clock to output port delay

tfco_max : Maximum clock to ouput delay from falling edge (external device) falling edge external device maximum clock to output port delay

trce_dly_min : (Minimum board trace delay) minimum board trace delay

trce_dly_max : (Maximum board trace delay) maximum board trace delay

dv_bre : (Data valid before the rising clock edge) The minimum valid time of data before the rising edge of the clock

dv_are : (Data valid after the rising clock edge) The minimum valid time of data after the rising edge of the clock

dv_bfe : (Data valid before the falling clock edge) The minimum valid time of data before the falling edge of the clock

dv_afe : (Data valid after the falling clock edge) The minimum valid time of data after the falling edge of the clock

skew_bre : (Data invalid before the rising clock edge) the maximum invalid time of data before the rising edge of the clock

skew_are : (Data invalid after the rising clock edge) the maximum invalid time of data after the rising edge of the clock

skew_bfe : (Data invalid before the falling clock edge) the maximum invalid time of data before the falling edge of the clock

skew_afe : (Data invalid after the falling clock edge) the maximum invalid time of data after the falling edge of the clock

6.3.2 set_output_delay

set_output_delay command specifies the delay of the output path on the output port at the design interface relative to a certain clock edge. The command format is as follows:

set_output_delay

-clock <clock_name>

[-clock_fall]

[-rise] [-fall]

[-max] [-min]

[-add_delay]

[-source_latency_included]

<delay_value>

<port_list>

[-disable]

-clock : Indicates the name of its associated launch clock. When using clock , you need to follow the principle of declaration before use, that is: clock needs to be created by create_generated_clock or create_clock first .

[-clock_fall] : Indicates that only the falling edge of the trigger clock is considered.

[-rise] : That is, only consider the case where the input signal at the output is a rising edge.

[-fall] : Only consider the case where the input signal at the output is a falling edge.

Note: If the user does not define both, then the software will consider the rise or fall of the input signal at the output at the same time.

[-max] : Indicates that the user-defined delay value is the maximum value.

[-min] : Indicates that the user-defined delay value is the minimum value.

Note: If neither is defined by the user, the software will use the user-defined delay value in both the maximum and minimum delay analysis.

[-add_delay] : If the user has set_output_delay constraint on the output port before , then adding this option means that the software will retain the previously set constraint value. For the case of -max , the delay value will use the same value when calculating The case is calculated by the maximum value of all values, and for the case of -min , the calculation will be performed by the minimum value of all values in the same case.

[-source_latency_included] : Indicates that the delay value (the delay of the data path) has been subtracted from the clock source delay of the timing path. In this case, relative to the delay value, the delay value of the clock source of the clock path is 0 . If this option is not included, the source latency of the clock path needs to be specified in front of set_clock_latency . If not specified, then defaults to 0 .

<delay_value> : delay value, which is a floating point number.

<port_list> : output port , the user must get it through get_ports .

[-disable] : Make this constraint ineffective.

Note: The calculation method of the delay value parameter of the set_output_delay command is related to the synchronization method of the output data. Next, the calculation under the system synchronization and source synchronization interfaces will be introduced respectively.

System Synchronous Interface (System Synchronous Interface): Both the sending end and the receiving end are driven by a common system clock, which is called system synchronous input (system synchronous input). The clock signal of the system synchronous interface is completely synchronized by the system board level, and the data transmission delay It cannot be determined at this time and is not suitable for high-speed data transmission.

Under the system synchronization interface, there is only setup / hold mode (based on the FPGA external data valid window timing characteristics when calculating parameters), which are divided into three types: rising edge, falling edge, and double edge according to data speed and capture edge:

setup / hold mode is to set the output delay designed by the user according to the target device's setup and hold time requirements and considering the delay of the board traces or connecting lines, using the setup / hold mode constraint calculation formula.

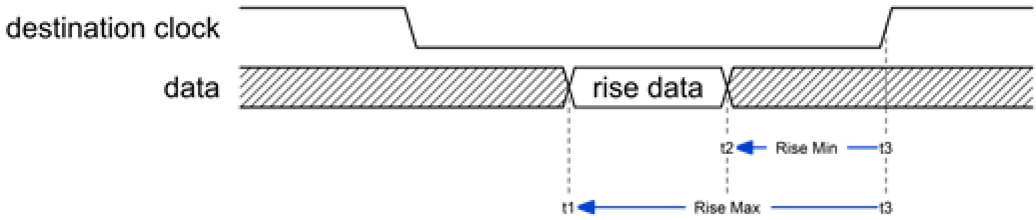


Figure 6-26 System Setup/Hold Rise Waveform Diagram

Rise Min = trce_dly_min - thd

Rise Max = trce_dly_max + tsu

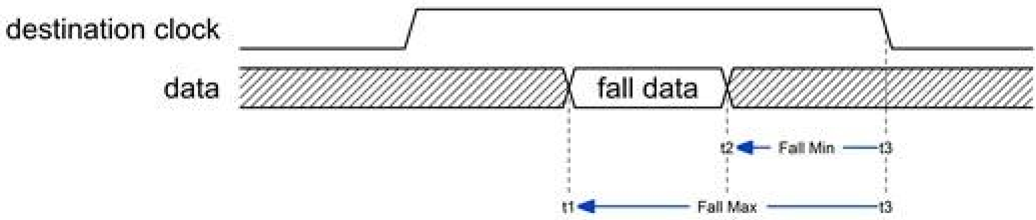


Figure 6-27 System Setup/Hold Fall Waveform Diagram

Fall Min = trce_dly_min - thd

Fall Max = trce_dly_max + tsu

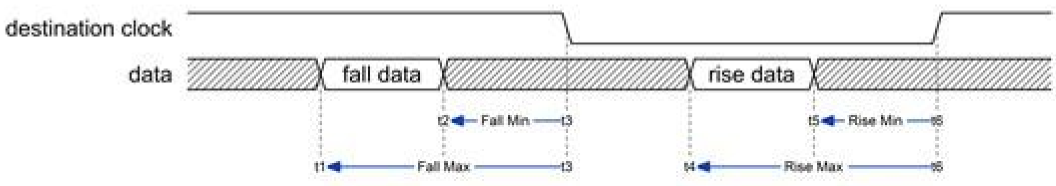


Figure 6-28 System Setup/Hold Dual Waveform Diagram

Rise Min = trce_dly_min - thd_r

Rise Max = trce_dly_max + tsu_r

Fall Min = trce_dly_min - thd_f

Fall Max = trce_dly_max + tsu_f

Source Synchronous Interface (Source Synchronous Interface): When the sender sends data, it sends a clock signal of the same source as the input data at the same time, and the output data and clock maintain a definite phase relationship, which can support high-speed data transmission.

Under the source synchronous interface, there are setup / hold mode (based on FPGA external data valid window timing characteristics when calculating parameters) and clock skew mode (based on FPGA output port clock skew requirements when calculating parameters), which are divided according to data speed and capture edge. There are three types: rising edge, falling edge and double edge:

Setup / hold mode (based on FPGA external data valid window timing characteristics when calculating parameters)

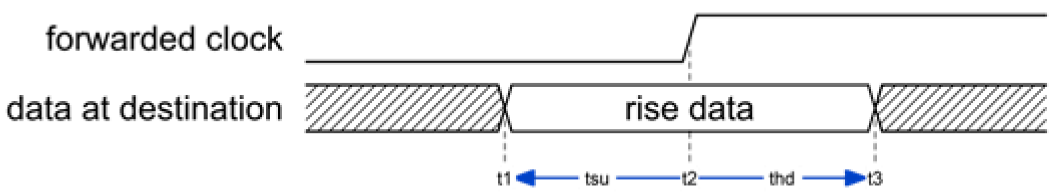


Figure 6-29 Source Setup/Hold Rise Waveform Diagram

Rise Min = trce_dly_min - thd

Rise Max = trce_dly_max + tsu

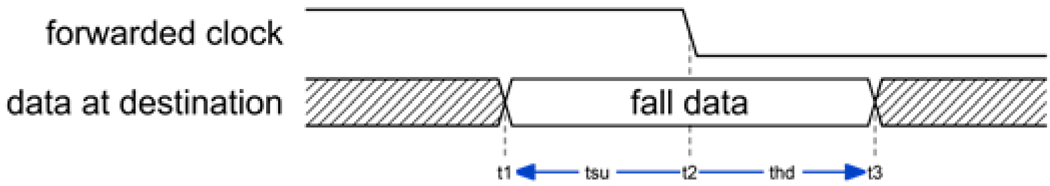


Figure 6-30 Source Setup/Hold Fall Waveform Diagram

Fall Min = trce_dly_min - thd

Fall Max = trce_dly_max + tsu



Figure 6-31 Source Setup/Hold Dual Waveform Diagram

Rise Min = trce_dly_min - thd_r

Rise Max = trce_dly_max + tsu_r

Fall Min = trce_dly_min - thd_f

Fall Max = trce_dly_max + tsu_f

The clock skew mode is given the clock skew of the user design data relative to the associated clock, and confirms whether the output delay meets the conditions. At this time, the clock skew mode constraint calculation formula is used.

Mode (based on FPGA output port clock skew requirements when calculating parameters)

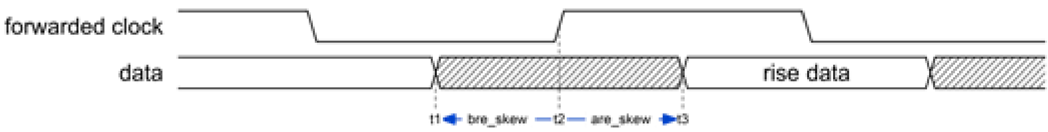


Figure 6-32 Source Skew Rise Waveform Diagram

Rise Min = bre_skew

Rise Max = period - are_skew

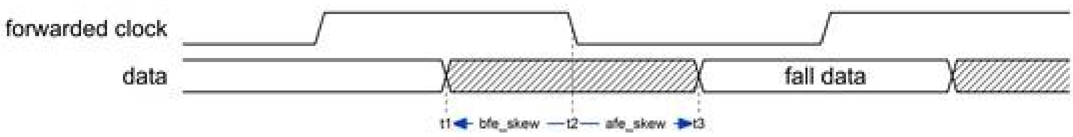


Figure 6-33 Source Skew Fall Waveform Diagram

Fall Min = bfe_skew

Fall Max = period – afe_skew

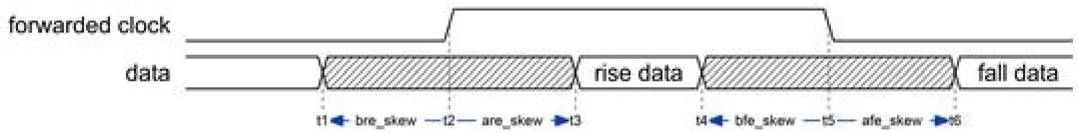


Figure 6-34 Source Skew Dual Waveform Diagram

Rise Min = bfe_skew

Rise Max = (period/2) – afe_skew

Fall Min = bre_skew

Fall Max = (period/2) – are_skew

The detailed meanings of the abbreviations in the calculation expressions are as follows:

tsu : (Destination device setup time requirement) target device setup time requirement

tsu_r : (Destination device setup time requirement for rising edge) target device setup time requirement for rising edge

tsu_f : (Destination device setup time requirement for falling edge) target device setup time requirement for falling edge

thd : (Destination device hold time requirement) target device hold time requirement

thd_r : (Destination device hold time requirement for rising edge) Target device hold time requirement for rising edge

thd_f : (Destination device hold time requirement for falling edge) target device hold time requirement for falling edge

bre_skew : (Skew requirement before rising edge) clock skew requirement before rising edge

bfe_skew : (Skew requirement before falling edge) clock skew requirement before falling edge

are_skew : (Skew requirement after rising edge) Clock skew requirement after rising edge

afe_skew : (Skew requirement after falling edge) clock skew requirement after falling edge

trce_dly_min : (Minimum board trace delay) minimum board trace delay

trce_dly_max : (Maximum board trace delay) maximum board trace delay

6.4 Assertions constraint command

6.4.1 set_max_skew

This command is used to constrain the maximum skew between a set of user-specified paths . The start point and end point of the constrained path must meet the requirements of startpoint and endpoint . set_max_skew is often used for gray code transmission, configuration registers, and multi-bit clock crossing implementations with CE/MUX/MUX hold circuits. When set_false_path or set_clock_groups is set , set_max_skew will be ignored; and when set_max_delay , set_min_delay , and set_multicycle_path are set , set_max_skew is still valid and will not conflict with their priorities.

set_max_skew :

[-from <from_list> | -rise_from <rise_from_list> | -fall_from <fall_from_list>]

[-through through_list]*

[-to <to_list> | -rise_to <rise_to_list> | -fall_to <fall_to_list>]

<skew_value>

[-disable]

The meaning of each parameter in the command is explained as follows. The square brackets indicate that the parameter is an optional value, the angle brackets indicate the parameter value or parameter list, * indicates that the parameter can be repeated, | indicates the or symbol, and multiple options at the same level can only use one :

[-from] : from_list indicates the startpoint of the path . Note that the startpoint must be one of the following types of points :

1. Clock , obtained through get_clocks , needs to follow the principle of declaration before use, that is: clock needs to be created through create_generated_clock or create_clock first ; if clock is defined , then startpoint is the clock pin of all registers that the clock network can fanout to , or It is all the inputs related to the clock (set_input_delay in the user sdc , otherwise the startpoint is invalid).

2. The io port , input or inout , can be obtained through get_ports .

3. The timing unit, obtained through get_cells , represents the clock pin of all timing units .

4. The clock pin of the sequential unit is obtained through get_pins .

[-rise_from] : This option can only be specified as clocks , indicating that the starting point of the timing path is triggered by the rising edge of the clock, where the rising edge of the clock refers to the rising edge of the clock definition point.

[-fall_from] : This option can only be specified as clocks , indicating that the starting point of the timing path is triggered by the falling edge of the clock, where the falling edge of the clock refers to the falling edge of the clock definition point.

Note: Three or symbols are used in the format definition, as follows:

[-from from_list | -rise_from rise_from_list | -fall_from fall_from_list] means -from from_list , -rise_from rise_from_list , -fall_from fall_from_list can only use any one of them.

[-to] : to_list indicates the endpoint of the path . Note that the endpoint must be one of the following types of points :

1. Clock , obtained through get_clocks , needs to follow the principle of declaration before use, that is: clock needs to be created through create_generated_clock or create_clock first ; if clock is defined , then the endpoint corresponds to the clock pins of all registers that the clock network can fanout to The data pin of the clock , or all outputs related to the clock (set_output_delay in the user sdc , otherwise the endpoint is invalid).

2. io port , output or inout , obtained through get_ports .

3. Sequential cells, obtained through get_cells , represent the data pins of all sequential cells .

4. The data pin of the sequential unit is obtained through get_pins .

[-rise_to] : This option can only be specified as clocks , indicating that the end of the timing path is triggered by the rising edge of the clock, where the rising edge of the clock refers to the rising edge of the clock definition point.

[-fall_to] : This option can only be specified as clocks , indicating that the end of the timing path is triggered by the falling edge of the clock, where the falling edge of the clock refers to the falling edge of the clock definition point.

Note: Three or symbols are used in the format definition, as follows:

[-to to_list | -fall_to fall_to_list | -rise_to rise_to_list] means -to to_list , -fall_to fall_to_list , -rise_to rise_to_list can only use any one of them.

[-through] : through_list indicates the intermediate points that the path must pass through.

Note: [-through through_list] * parameters are followed by * , indicating that this parameter can be repeated.

<skew_value> : Specifies the maximum skew value of a group of paths constrained by this command , in ns .

[-disable] : Make this constraint ineffective.

6.5 Exception constraint command

6.5.1 set_max_delay

This command is used to specify the maximum delay that the user expects for a certain path , but it should be noted that the start point and end point of this path must meet the requirements of startpoint and endpoint . This command is an exception command, because in general, the maximum delay that can satisfy the setup check is determined according to the delay of the clock path, the clock cycle and the constraint value of the setup check, and if the user specifies set_max_delay , then it can be Whether it meets the user's requirements has nothing to do with the clock path, clock cycle, and the constraint value of the setup check, as long as the delay from the data from the startpoint to the endpoint is less than the maximum value of the user's constraint.

the set_max_delay command is as follows:

set_max_delay:

[-from <from_list> | -rise_from <rise_from_list> | -fall_from <fall_from_list>]

[-through <through_list>]*

[-to <to_list> | -rise_to <rise_to_list> | -fall_to <fall_to_list>]

[-datapath_only]

<delay_value>

[-disable]

The meaning of each parameter in the command is explained as follows. The square brackets indicate that the parameter is an optional value, the angle brackets indicate the parameter value or parameter list, * indicates that the parameter can be repeated, | indicates the or symbol, and multiple options at the same level can only use one :

[-from] : from_list indicates the startpoint of the path . Note that startpoint must be one of the following types of points :

① clock : Obtained by get_clocks , if the clock is defined , then the startpoint is the clock pin of all registers that the clock network can fanout to , or all the inputs related to the clock (set_input_delay in the user sdc , otherwise the startpoint is invalid), when using clock , you need to follow the principle of declaration before use, that is: clock needs to be created by create_generated_clock or create_clock first .

② io port : input or inout , obtained through get_ports (note: the input or inout must be a port that defines set_input_delay , otherwise the startpoint is invalid).

unit: Obtained through get_cells , indicating the clock pin of all sequential units .

clock pin of the sequential unit : obtained through get_pins .

[-rise_from] : This option can only be specified as clocks , indicating that the starting point of the timing path is triggered by the rising edge of the clock, where the rising edge of the clock refers to the rising edge of the clock definition point.

[-fall_from] : This option can only be specified as clocks , indicating that the starting point of the timing path is triggered by the falling edge of the clock, where the falling edge of the clock refers to the falling edge of the clock definition point.

[-to] : to_list indicates the endpoint of the path . Note that the endpoint must be one of the following types of points :

① clock : Obtained through get_clocks . If clock is defined , then the endpoint is the data pin corresponding to the clock pins of all registers that the clock network can fanout to, or all outputs related to the clock (set by set_output_delay in the user sdc) specified , otherwise the endpoint is invalid), when using clock , you need to follow the principle of declaration before use, that is: clock needs to be created by create_generated_clock or create_clock first .

② io port : output or inout , obtained through get_ports (note: the output or inout must be a port that defines set_output_delay , otherwise the endpoint is invalid).

unit: Obtained through get_cells , indicating the data pin of all sequential units .

data pin of the sequential unit : obtained through get_pins .

[-rise_to] : This option can only be specified as clocks , indicating that the end of the timing path is triggered by the rising edge of the clock, where the rising edge of the clock refers to the rising edge of the clock definition point.

[-fall_to] : This option can only be specified as clocks , indicating that the end of the timing path is triggered by the falling edge of the clock, where the falling edge of the clock refers to the falling edge of the clock definition point

-through through_list : through_list indicates the intermediate points that the path must pass through. Consider that the polarity of the signal may change during transmission, such as a NOT gate. In addition, the following two parameters are provided, and the intermediate point must be one of the following types of points :

Note: [-through through_list] * parameters are followed by * , indicating that this parameter can be repeated.

① Combination unit: Obtained through get_cells , which means any input pin of the combination unit .

②The input of the combination unit : obtained through get_pins .

③ net : Obtained through get_nets , indicating that the path will pass through the driver pin of this net .

[-datapath_only] : Indicates that the specified max delay path does not care about the skew and jitter of the clock, and only considers the data path , including the CLK -> Q delay of the first trigger, the setup time of the second trigger , and two Combined path delay between triggers. Note: If a max delay path is set to datapath_only , since the skew and jitter of the clock are not considered, the hold path of this path will not be analyzed.

<delay_value> : delay value, a floating point number

[-disable] : Make this constraint ineffective.

The command is as follows:

#The maximum delay of all paths from the Q terminal of flip-flop UFF2 to the D terminal of flip-flop UFF3 is 0.6ns

set_max_delay 0.6 –from UFF2/Q –to UFF3/D

#The maximum delay of all paths between the SYS_CLK and CFG_CLK clock domains is 1.2ns

set_max_delay 1.2 -from [get_clocks SYS_CLK] -to [get_clocks CFG_CLK]

#The maximum delay of all data paths from the Q terminal of flip-flop UFF2 to the D terminal of flip-flop UFF3 is 0.6ns , regardless of clock skew and jitter .

set_max_delay 0.6 –from UFF2/Q –to UFF3/D –datapath_only

6.5.2 set_min_delay

This command is used to specify the minimum delay that the user expects for a certain path . The start point and end point of this path must meet the requirements of startpoint and endpoint . This command is an exception command, because in general, the minimum delay that can satisfy the hold check is determined according to the delay of the clock path and the constraint value of the hold check, and if the user specifies set_min_delay , can the user be satisfied at this time? The requirement has nothing to do with the clock path and the constraint value of the hold check, as long as the delay from the data from the startpoint to the endpoint is greater than the minimum value constrained by the user.

the set_min_delay command is as follows:

set_max_delay:

[-from from_list]

[-rise_from from_list]

[-fall_from from_list]

[-through through_list]*

[-to to_list]

[-rise_to_list]

[-fall_to_list]

<delay_value>

[-disable]

The meaning of each parameter in the command is explained as follows. The square brackets indicate that the parameter is an optional value, the angle brackets indicate the parameter value or parameter list, * indicates that the parameter can be repeated, | indicates the or symbol, and multiple options at the same level can only use one :

[-from] : from_list indicates the startpoint of the path . Note that the startpoint must be one of the following types of points :

① clock : Obtained by get_clocks , if the clock is defined , then the startpoint is the clock pin of all registers that the clock network can fanout to , or all the inputs related to the clock (set_input_delay in the user sdc , otherwise the startpoint is invalid), when using clock , you need to follow the principle of declaration before use, that is: clock needs to be created by create_generated_clock or create_clock first .

② io port : input or inout , obtained through get_ports (note: the input or inout must be a port that defines set_input_delay , otherwise the startpoint is invalid).

unit: Obtained through get_cells , indicating the clock pin of all sequential units .

clock pin of the sequential unit : obtained through get_pins .

[-rise_from] : This option can only be specified as clocks , indicating that the starting point of the timing path is triggered by the rising edge of the clock, where the rising edge of the clock refers to the rising edge of the clock definition point.

[-fall_from] : This option can only be specified as clocks , indicating that the starting point of the timing path is triggered by the falling edge of the clock, where the falling edge of the clock refers to the falling edge of the clock definition point.

[-to] : to_list indicates the endpoint of the path . Note that the endpoint must be one of the following types of points :

① clock : Obtained through get_clocks . If clock is defined , then the endpoint is the data pin corresponding to the clock pins of all registers that the clock network can fanout to, or all outputs related to the clock (set by set_output_delay in the user sdc) specified , otherwise the endpoint is invalid), when using clock , you need to follow the principle of declaration before use, that is: clock needs to be created by create_generated_clock or create_clock first .

② io port : output or inout , obtained through get_ports (note: the output or inout must be a port that defines set_output_delay , otherwise the endpoint is invalid).

unit: Obtained through get_cells , indicating the data pin of all sequential units .

data pin of the sequential unit : obtained through get_pins .

[-rise_to] : This option can only be specified as clocks , indicating that the end of the timing path is triggered by the rising edge of the clock, where the rising edge of the clock refers to the rising edge of the clock definition point.

[-fall_to] : This option can only be specified as clocks , indicating that the end of the timing path is triggered by the falling edge of the clock, where the falling edge of the clock refers to the falling edge of the clock definition point.

-through through_list* : through_list indicates the intermediate points that the path must pass through.

Note: [-through through_list] * parameters are followed by * , indicating that this parameter can be repeated.

<delay_value> : delay value, a floating point number

[-disable] : Make this constraint ineffective.

The command is as follows:

#The minimum delay of all paths from the Q terminal of flip-flop UFF2 to the D terminal of flip-flop UFF3 is 0.15ns

Set_min_delay 0.15 –from UFF2/Q –to UFF3/D

#The minimum delay of all paths between the SYS_CLK and CFG_CLK clock domains is 1.2ns

set_min_delay 0.4 -from [get_clocks SYS_CLK] -to [get_clocks CFG_CLK]

6.5.3 set_multicycle_path

the set_multicycle_path command is as follows:

set_multicycle_path:

[-from from_list]

[-rise_from from_list]

[-fall_from from_list]

[-through through_list]*

[-to to_list]

[-rise_to_list]

[-fall_to_list]

[-start] [-end]

[-setup] [-hold]

<path_multiplier>

[-disable]

The meaning of each parameter in the command is explained as follows. The square brackets indicate that the parameter is an optional value, the angle brackets indicate the parameter value or parameter list, * indicates that the parameter can be repeated, | indicates the or symbol, and multiple options at the same level can only use one :

[-setup] : Indicates that the clock cycle uses the specified multiple during setup analysis. After Setup is specified, hold will also be affected. By default, setup is used .

[-hold] : Indicates that when hold analysis, the clock cycle uses the specified multiple.

[-start] : Indicates that this multi-cycle setting is related to the launch clock . Assuming that the number of cycles set by the command is N , then for the setup , the launch clock needs to use the edge at the first N-1 cycles of the default analysis edge (The edge of the hold analysis also moves); for hold , the edge at the last N cycles of the edge is analyzed by default using the launch clock . Generally used in the fast to slow clock domain, as shown in the figure below: As shown in the figure below:

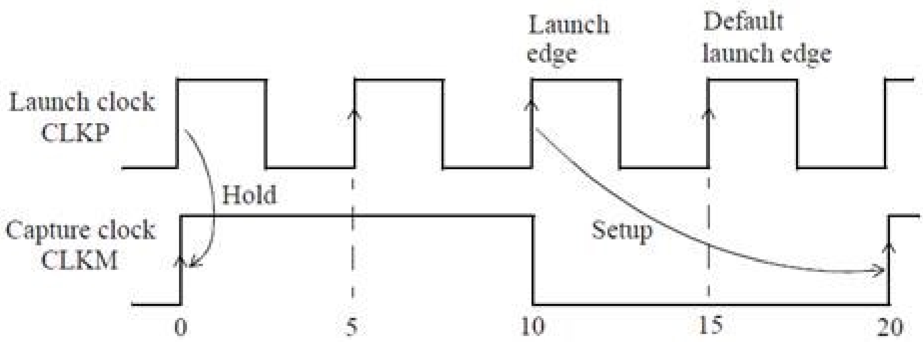


Figure 6-35 Set Multicycle Path example (start)

The default timing analysis edge pair in the figure above is setup : launch clock 15 , capture clock 20 ; hold : launch clock 0 , capture clock 0 . If you want to set the edge of the launch clock at 10 for the setup analysis (the launch clock is one cycle ahead), you can write like this:

set_multicycle_path 2 -setup -from [get_clocks CLKP] -to [get_clocks CLKM] –start

This command means: This command sets the setup and start options, that is, it needs to analyze the edge at the previous period of the default analysis edge of the launch clock (the hold edge will

also change accordingly). After setting this command, the edge pairs for timing analysis are setup : launch clock 10 , capture clock 20 ; hold : launch clock 15 , capture clock 20 . If you need to hold the edge analysis shown in the figure, you also need to move the hold analysis edge of the launch clock back by one cycle, which can be achieved by the following command:

set_multicycle_path 1 -hold -from [get_clocks CLKP] -to [get_clocks CLKM] -start

Based on the previous command, this command moves the edge of the hold analysis back one cycle in the launch clock (setup does not move), and the result is hold : launch clock 0 , capture clock 0 . (launch 20 , capture 20 and launch 0 , capture 0 in the figure are the same edge pair).

[-end] : Indicates that this multi-cycle setting is related to the capture clock . Assuming that the number of cycles set by the command is N , then for the setup , the capture clock needs to use the edge at the last N-1 cycle of the default analysis edge (The edge of the hold analysis also moves); for hold , the edge at the first N cycles of the edge is analyzed by default using the capture clock . Generally used in the slow to fast clock domain, as shown in the following figure:

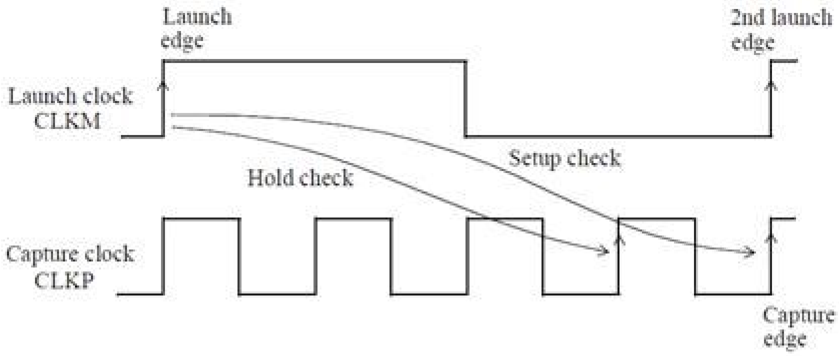


Figure 6-36 Set Multicycle Path Example (end)

of the default setup analysis in the above figure is the first rising edge of the launch clock in the figure and the second rising edge of the capture clock , and the edge pair of the hold analysis is the first rising edge of the launch clock in the figure edge and the first rising edge of the capture clock . If you want to change to the edge pair analysis as shown in the figure, you need to move the edges of the setup and hold analysis of the capture clock backward by 3 clock cycles. Since the hold will move after the setup is moved , you can add the following command to achieve:

set_multicycle_path 4 -setup -from [get_clocks CLKM] -to [get_clocks CLKP] -end

[-from] : from_list indicates the startpoint of the path . Note that the startpoint must be one of the following types of points :

① clock : Obtained by get_clocks , if the clock is defined , then the startpoint is the clock pin of all registers that the clock network can fanout to , or all the inputs related to the clock (set_input_delay in the user sdc , otherwise the startpoint is invalid), when using clock , you need to follow the principle of declaration before use, that is: clock needs to be created by create_generated_clock or create_clock first .

② io port : input or inout , obtained through get_ports (note: the input or inout must be a port that defines set_input_delay , otherwise the startpoint is invalid).

unit: Obtained through get_cells , indicating the clock pin of all sequential units .

clock pin of the sequential unit : obtained through get_pins .

[-rise_from] : This option can only be specified as clocks , indicating that the starting point of the timing path is triggered by the rising edge of the clock, where the rising edge of the clock refers to the rising edge of the clock definition point.

[-fall_from] : This option can only be specified as clocks , indicating that the starting point of the timing path is triggered by the falling edge of the clock, where the falling edge of the clock refers to the falling edge of the clock definition point.

[-to] : to_list indicates the endpoint of the path . Note that the endpoint must be one of the following types of points :

① clock : Obtained through get_clocks . If clock is defined , then the endpoint is the data pin corresponding to the clock pins of all registers that the clock network can fanout to, or all outputs related to the clock (set by set_output_delay in the user sdc) Otherwise, the endpoint is invalid), when using clock , you need to follow the principle of declaration before use, that is: clock needs to be created by create_generated_clock or create_clock first .

② io port : output or inout , obtained through get_ports (note: the output or inout must be a port that defines set_output_delay , otherwise the endpoint is invalid).

unit: Obtained through get_cells , indicating the data pin of all sequential units .

data pin of the sequential unit : obtained through get_pins .

[-rise_to] : This option can only be specified as clocks , indicating that the end of the timing path is triggered by the rising edge of the clock, where the rising edge of the clock refers to the rising edge of the clock definition point.

[-fall_to] : This option can only be specified as clocks , indicating that the end of the timing path is triggered by the falling edge of the clock, where the falling edge of the clock refers to the falling edge of the clock definition point.

[-through] : through_list indicates the intermediate points that the path must pass through.

Note: [-through <through_list>] * parameters are followed by * , indicating that this parameter can be repeated.

<path_multiplier> : Indicates the number of cycles to be set, which is an integer greater than or equal to 0 . When set to 0 , it means that the specified path is zero cycle path .

[-disable] : Make this constraint ineffective.

6.5.4 set_false_path

set_false_path command format

As follows:

set_false_path:

[-from <from_list> | -rise_from <rise_from_list> | -fall_from <fall_from_list>]

[-through through_list]*

[-to <to_list> | -rise_to <rise_to_list> | -fall_to <fall_to_list>]

[-setup] [-hold]

[-disable]

The meaning of each parameter in the command is explained as follows. The square brackets indicate that the parameter is an optional value, the angle brackets indicate the parameter value or parameter list, * indicates that the parameter can be repeated, | indicates the or symbol, and multiple options at the same level can only use one :

[-setup] : Indicates that the setup analysis is performed

[-hold] : Indicates that the hold analysis is performed

[-from] : from_list indicates the startpoint of the path . Note that the startpoint must be one of the following types of points :

① clock : Obtained by get_clocks , if the clock is defined , then the startpoint is the clock pin of all registers that the clock network can fanout to , or all the inputs related to the clock (set_input_delay in the user sdc , otherwise the startpoint is invalid), when using clock , you need to

follow the principle of declaration before use, that is: clock needs to be created by create_generated_clock or create_clock first .

② io port : input or inout , obtained through get_ports (note: the input or inout must be a port that defines set_input_delay , otherwise the startpoint is invalid).

unit: Obtained through get_cells , indicating the clock pin of all sequential units .

clock pin of the sequential unit : obtained through get_pins .

[-rise_from] : This option can only be specified as clocks , indicating that the starting point of the timing path is triggered by the rising edge of the clock, where the rising edge of the clock refers to the rising edge of the clock definition point.

[-fall_from] : This option can only be specified as clocks , indicating that the starting point of the timing path is triggered by the falling edge of the clock, where the falling edge of the clock refers to the falling edge of the clock definition point.

[-to] : "to_list" indicates the endpoint of the path . Note that the endpoint must be one of the following types of points :

① clock : Obtained through get_clocks . If clock is defined , then the endpoint is the data pin corresponding to the clock pins of all registers that the clock network can fanout to, or all outputs related to the clock (set by set_output_delay in the user sdc) Otherwise, the endpoint is invalid) , when using clock , you need to follow the principle of declaration before use, that is: clock needs to be created by create_generated_clock or create_clock first .

② io port : output or inout , obtained through get_ports (note: the output or inout must be a port that defines set_output_delay , otherwise the endpoint is invalid).

unit: Obtained through get_cells , indicating the data pin of all sequential units .

data pin of the sequential unit : obtained through get_pins .

[-rise_to] : This option can only be specified as clocks , indicating that the end of the timing path is triggered by the rising edge of the clock, where the rising edge of the clock refers to the rising edge of the clock definition point.

[-fall_to] : This option can only be specified as clocks , indicating that the end of the timing path is triggered by the falling edge of the clock, where the falling edge of the clock refers to the falling edge of the clock definition point.

[-through] : through_list indicates the intermediate points that the path must pass through.

[-disable] : Make this constraint ineffective.

Note: [-through through_list] * parameters are followed by * , indicating that this parameter can be repeated.

Constraint save files are saved in different file types depending on whether the synthesis tool is used. When the synthesis tool (integrated version) is used, the constraints are saved in the constraint file (fdc) ; when the synthesis tool (backend version) is not used , the constraints are saved in the timing Constraints file (sdc) .

The command is as follows:

#Invalidate the timing path from ff12 to ff34

set_false_path -from ff12 -to ff34

#Invalidate the Hold check analysis of all endpoints driven by CLK1

set_false_path -hold -to [get_clocks CLK1]

6.6 Report command

6.6.1 Report_timing

report_timing

[-from from_list | -rise_from rise_from_list | -fall_from fall_from_list]

[-to to_list | -rise_to rise_to_list | -fall_to fall_to_list]

[-through through_list]*

[-delay_type delay_type]

[-nworst paths_per_endpoint]

[-max_path count]

[-from] : from_list indicates the startpoint of the path . Note that the startpoint must be one of the following types of points :

1. Clock , obtained through get_clocks , needs to follow the principle of declaration before use, that is: clock needs to be created through create_generated_clock or create_clock first ; if clock is defined , then startpoint is the clock pin of all registers that the clock network can fanout to , or It is

all the inputs related to the clock (set_input_delay in the user sdc , otherwise the startpoint is invalid).

2. The io port , input or inout , can be obtained through get_ports .

3. The timing unit, obtained through get_cells , represents the clock pin of all timing units .

4. The clock pin of the sequential unit is obtained through get_pins .

[-rise_from] : This option can only be specified as clocks , indicating that the starting point of the timing path is triggered by the rising edge of the clock, where the rising edge of the clock refers to the rising edge of the clock definition point.

[-fall_from] : This option can only be specified as clocks , indicating that the starting point of the timing path is triggered by the falling edge of the clock, where the falling edge of the clock refers to the falling edge of the clock definition point.

Note: Three or symbols are used in the format definition, as follows:

[-from from_list | -rise_from rise_from_list | -fall_from fall_from_list] means -from from_list , -rise_from rise_from_list , -fall_from fall_from_list can only use any one of them.

[-to] : to_list indicates the endpoint of the path . Note that the endpoint must be one of the following types of points :

1. Clock , obtained through get_clocks , needs to follow the principle of declaration before use, that is: clock needs to be created through create_generated_clock or create_clock first ; if clock is defined , then the endpoint corresponds to the clock pins of all registers that the clock network can fanout to The data pin of the clock , or all outputs related to the clock (set_output_delay in the user sdc , otherwise the endpoint is invalid).

2. io port , output or inout , obtained through get_ports .

3. Sequential cells, obtained through get_cells , represent the data pins of all sequential cells .

4. The data pin of the sequential unit is obtained through get_pins .

[-rise_to] : This option can only be specified as clocks , indicating that the end of the timing path is triggered by the rising edge of the clock, where the rising edge of the clock refers to the rising edge of the clock definition point.

[-fall_to] : This option can only be specified as clocks , indicating that the end of the timing path is triggered by the falling edge of the clock, where the falling edge of the clock refers to the falling edge of the clock definition point.

Note: Three or symbols are used in the format definition, as follows:

[-to to_list | -fall_to fall_to_list | -rise_to rise_to_list] means -to to_list , -fall_to fall_to_list , -rise_to rise_to_list can only use any one of them.

[-through] : through_list indicates the intermediate points that the path must pass through.

Note: [-through through_list] * parameters are followed by * , indicating that this parameter can be repeated.

-delay_type : Indicates the delay type of the path . There are three types, min , max , and min_max . Among them, min indicates that the analysis is carried out by hold analysis, and max indicates that this analysis is carried out by setup analysis, and min_max requires both setup and hold . analyze.

-nworst paths_per_endpoint : Indicates the number of paths to be reported for each endpoint of each path group .

-max_path count : The number of paths to report for each path group .

6.6 Command syntax

6.6.1 tcl command format

The following describes the command format of tcl :

Tcl command consists of the following parts:

[1] Commands is the command name, such as set_input_delay , a command can contain other subcommands, semicolon or newline as the end of the command. Subcommands end with a curly brace on the right, see subcommands below.

[2] Words are characters, and characters are separated by spaces.

[3] Double quotes are double quotes, which treat multiple characters as a string rather than a single character. Within the scope of double quotes, whether it is a semicolon, right curly brace, or a

space bar or a newline character will be treated as a character, subcommands, variables, and backslashes are still valid.

[4] Braces . That is, curly braces, all subcommands and variables will be treated as characters within the curly braces.

[5] Command substitution subcommands start with a left bracket and end with a right bracket.

[6] Variable substitution variable definition. Start with $. When parsing, the value of the variable will replace the variable.

[7] Backslash substitution is backslash. Like backslashes in C and other languages, backslashes in tcl are used in escape characters.

[8] Comments. Comments start with # .

6.6.2 List problem

Let's look at the writing methods of from_list , rise_from_list , fall_from_list , to_list , fall_to_list , rise_to_list , through_list , rise_through_list , fall_through_list . As mentioned above, they need to be obtained through commands such as get_pins , so they should be written according to the syntax of tcl :

set_min_delay -rise_through [get_ports clk]

If you want to get multiple ports , you can write like this:

set_min_delay -rise_from [get_ports {clk rst_n}] -rise_to [get_ports {clk1 rst_n1}]

If the list comes from the port and also from the pin , then it should be written separately, assuming that clk comes from the port , rst_n comes from the pin , and has the following relationship:

pin clk->port rst_n1 ;

pin clk->pin clk1 ;

port rst_n -> port rst_n1 ;

port rst_n -> pin clk1 ;

Four commands are required to support.

set_min_delay -rise_through [get_pins clk] -rise_through [get_ports rst_n1]

set_min_delay -rise_through [get_pins clk] -rise_through [get_pins clk1]

set_min_delay -rise_through [get_ports rst_n] -rise_through [get_pins clk1]

set_min_delay -rise_through [get_ports rst_n] -rise_through [get_ports rst_n1]

It can be seen that when there are multiple types of list objects, the required commands will increase exponentially, so when constraining, try to use the same type of list objects, such as using all pins for from and ports for to , instead of from or to use pin and port at the same time . The situation of other lists is the same and will not be described in detail.

7 Local dynamic reconfiguration

7.1 Enable dynamic reconfiguration

7.1.1 Operation demonstration

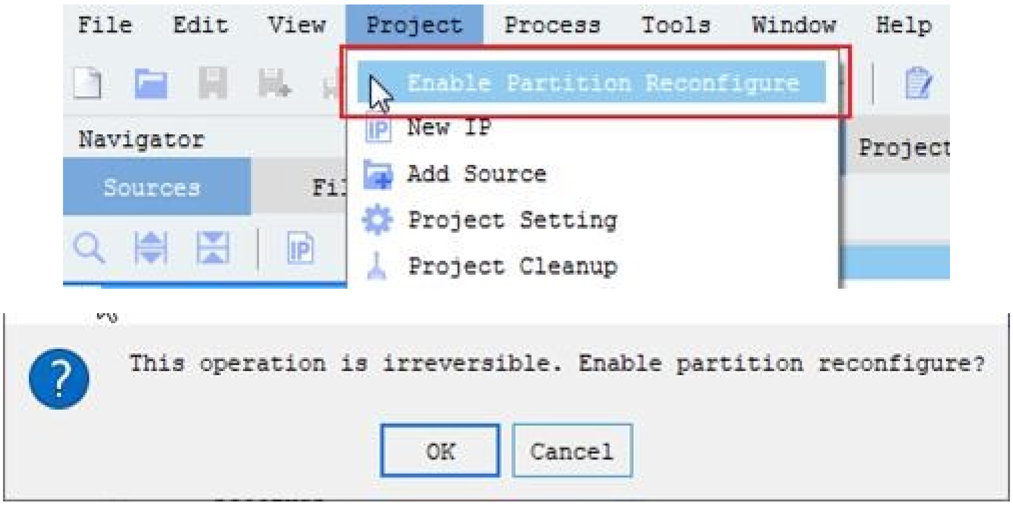


Figure 7-1 Start local dynamic reconfiguration

After the local dynamic reconfiguration mode is enabled for a project, the project cannot be restored to normal mode, but other projects are not affected, that is, this operation is irreversible on a project-by-project basis.

7.1.2 Interface description

After the local dynamic reconfiguration mode is enabled, compared with the normal mode, the PDS interface will add " Partition Definition " to the " Sources " component in the upper left corner, and " Multiple Flows " to the " Console " component.

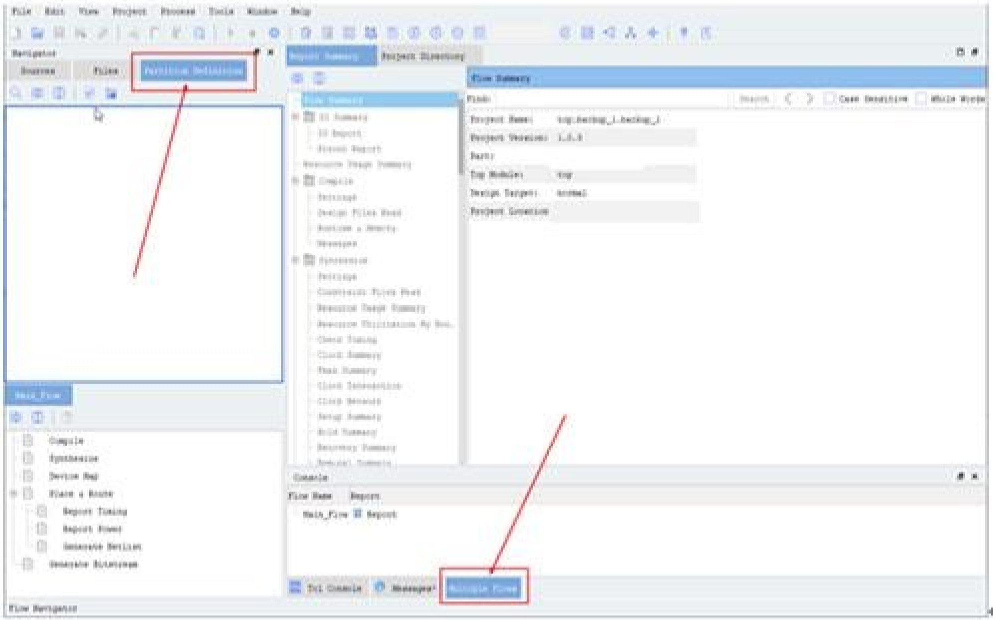


Figure 7-2 Interface display

7.2 Create Partition Definitions

7.2.1 Operation demonstration

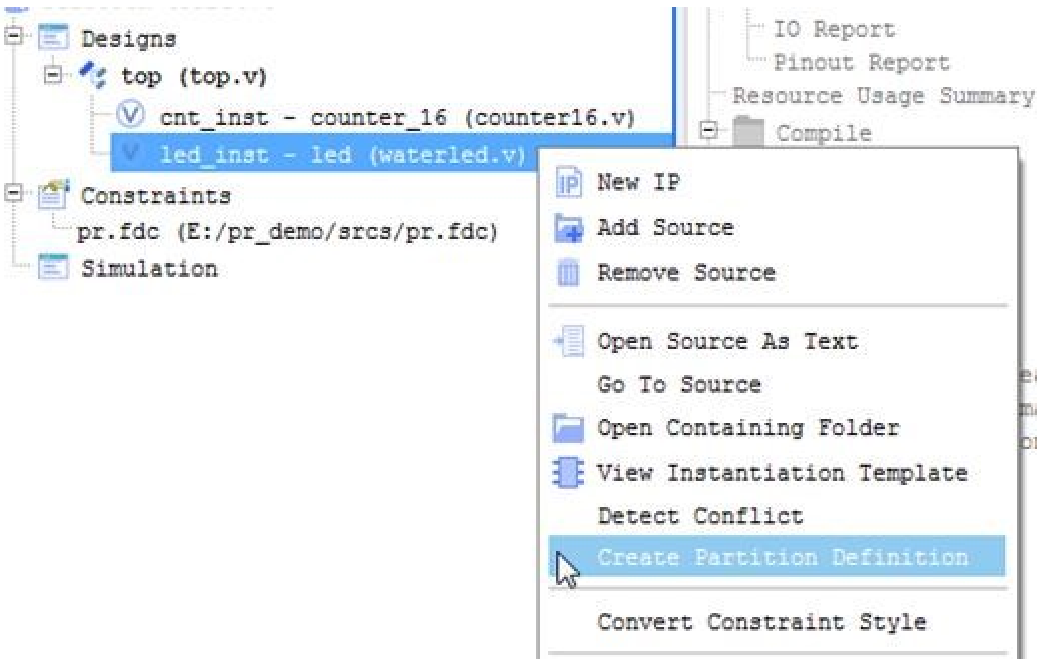


Figure 7-3 Create Partition Definition operation

Right-click the corresponding node in the Module Hierarchy of the " Sources " component , and select " Create Partition Definition ".

7.2.2 Interface description

Compared with normal mode, after partial dynamic reconfiguration is enabled, a " Partition Definition " component will be added to the " Navigator " component to display and manage the Module Hierarchy of PD , RM , and RM ; " Multiple Flows " will be added to the " Console " component Components for displaying, managing and operating processes. Subsequent chapters will describe each new component in more detail.

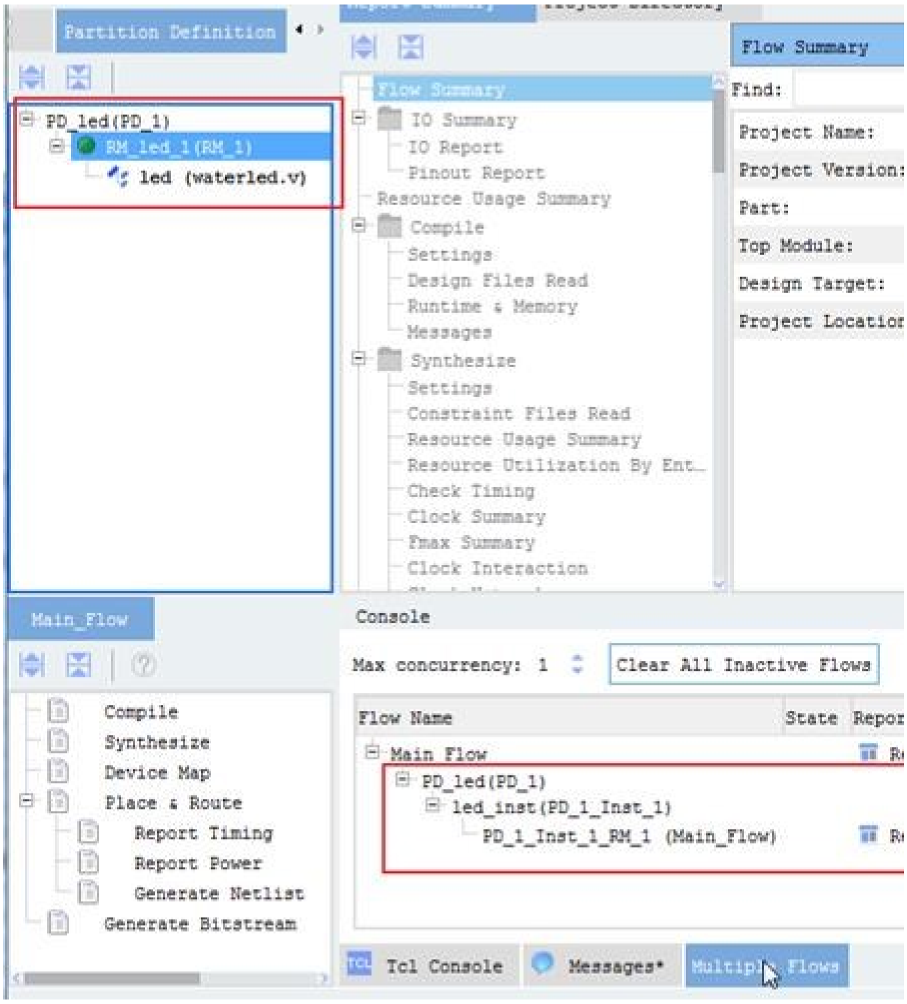


Figure 7-4 Interface Description

7.2.3 Partition Definition Instance icon

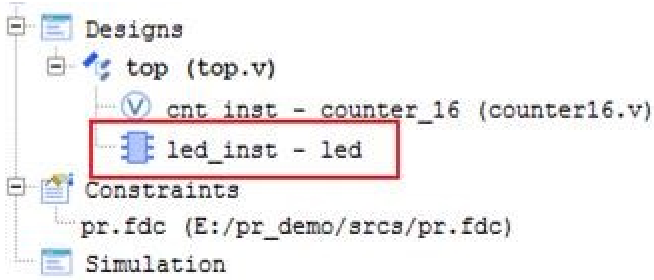


Figure 7-5 PD_led icon

led_inst is the Instance of PD " PD_led " , identified by the icon in the red box above.

7.2.4 Partition Definition

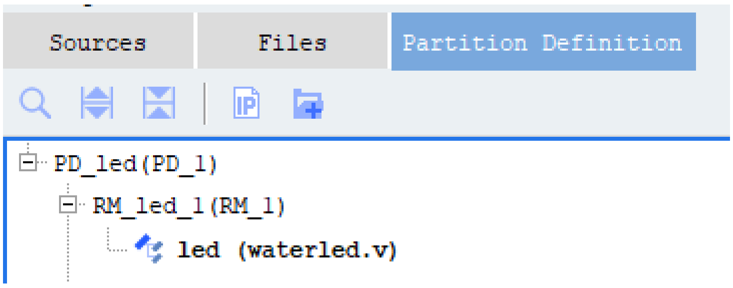


Figure 7-6 Partition Definition interface

PD (Partition Definition) is created , the PD , the RM (Reconfigure Module) managed by the PD , and the Module Hierarchy of the RM will be displayed in the " Partition Definition " section .

" PD_led " is the PD name, " RM_led " is the RM name; " PD_1 " is the PD index name, "RM_1" is the RM index name.

7.2.5 Default RM for PD

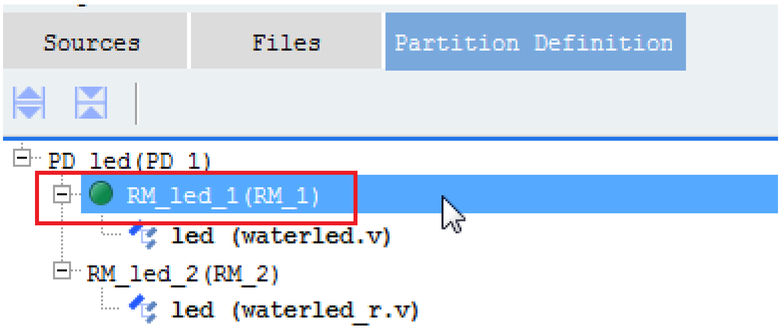


Figure 7-7 Default RM for PD

As shown in the figure above, RM_led_1 (RM_1) is the default RM of PD_led (PD_1) , identified by the icon in the red box.

When running the main process, the PD 's default RM will be configured for each PD 's Instance to run.

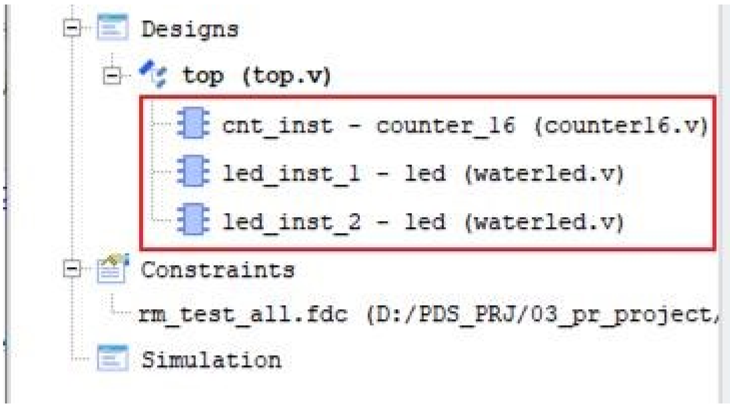


Figure 7-8 Process runtime

For example, in the example shown in the figure above, when running the main process, RM_led_1 (PD_1_RM_1) will be configured to two Instances of PD_led (PD_1) : led_inst_1 and led_inst_2 .

7.2.6 Multiple Flows

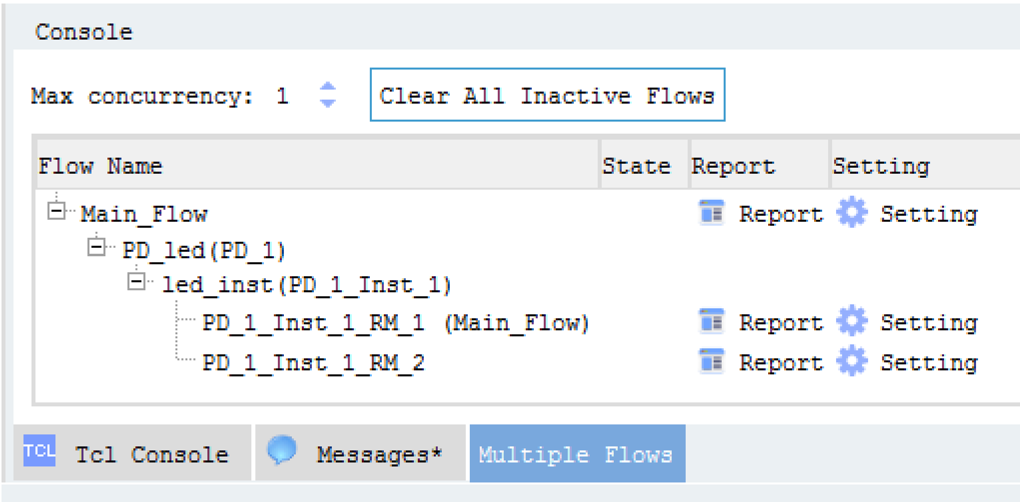


Figure 7-9 Multiple Flow window

" Main Flow " is the main process, that is, the complete process including the static area and the dynamic area; " PD_led " is the PD name, " led_inst " is the instance name of PD_led; " PD_1_Inst_1_RM_2 " is the partial reconfiguration process, meaning led_inst (PD_1_Inst_1) Select PD_1_RM_1 to run the process, that is, the instance led_inst of PD_led (PD_1) selects the RM_1 (RM_led_1) run process managed by PD_1 (PD_led).

7.2.7 Restrictions on creating PDs

(1) PD cannot be created for top module .

(2)

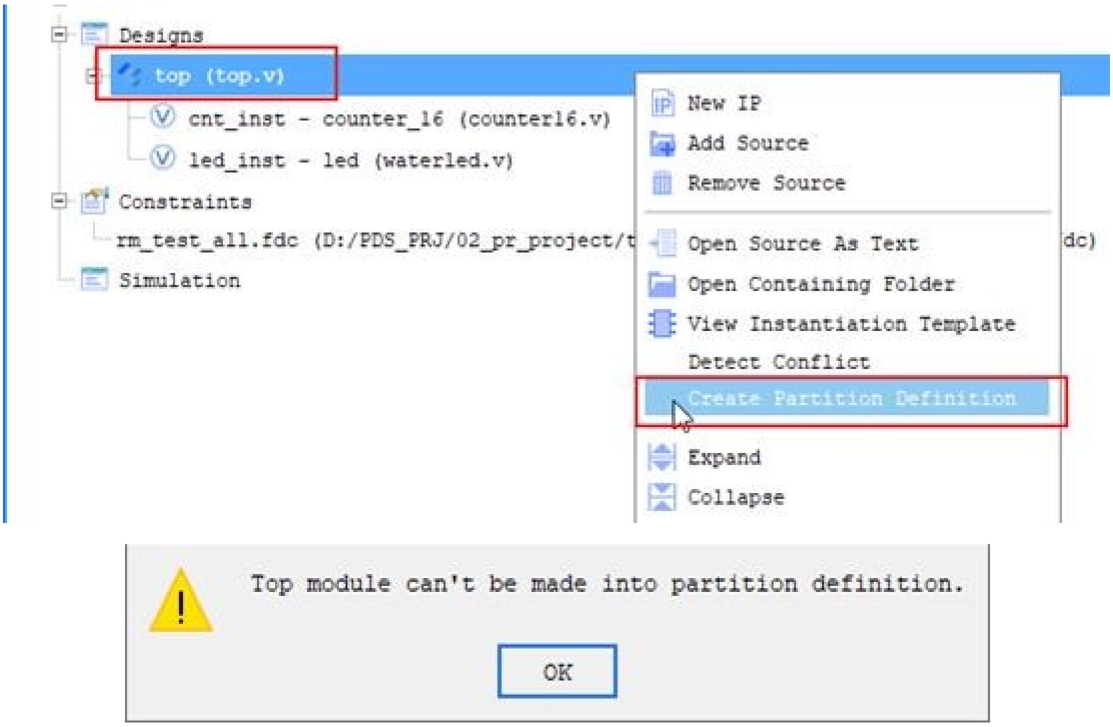


Figure 7-10 Do not operate 1

(3) PD cannot be created for the node of the inactive branch (that is, the top module of the branch is not the top module of the project) .

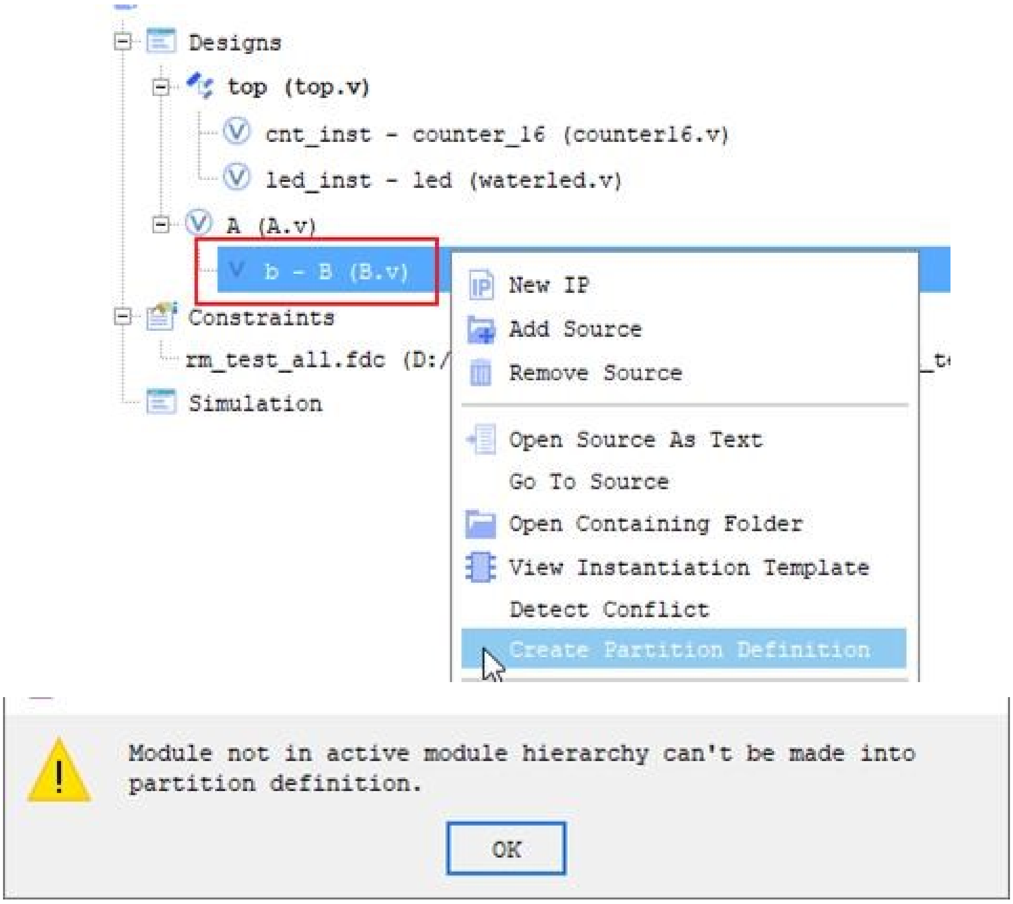


Figure 7-11 Do not operate 2

(4) Each design file where the module that needs to be created as a PD and all the modules under its hierarchy are located can only have one module definition.

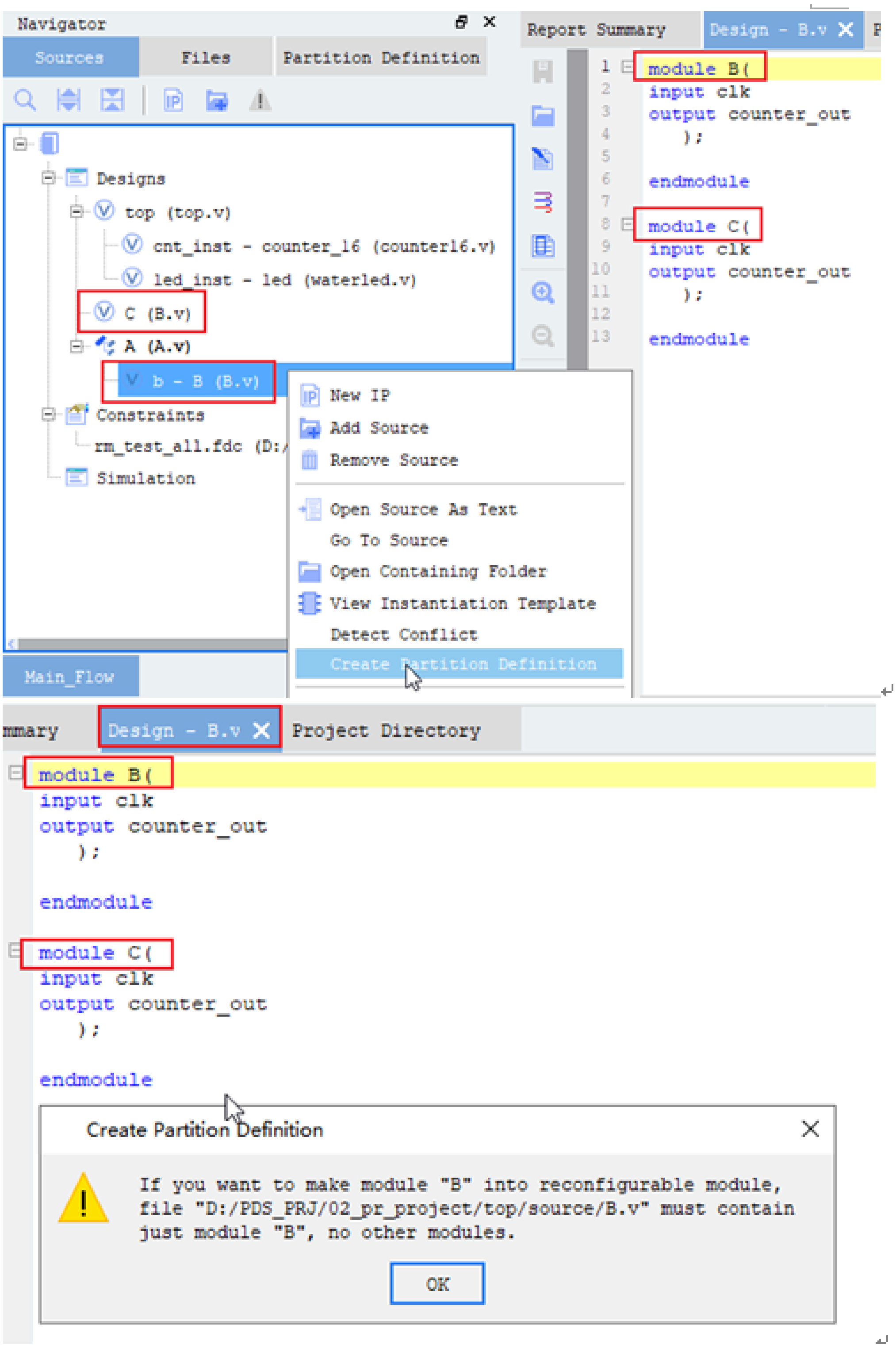


Figure 7-12 Do not operate 3

(5) IP cannot be created directly into PD .

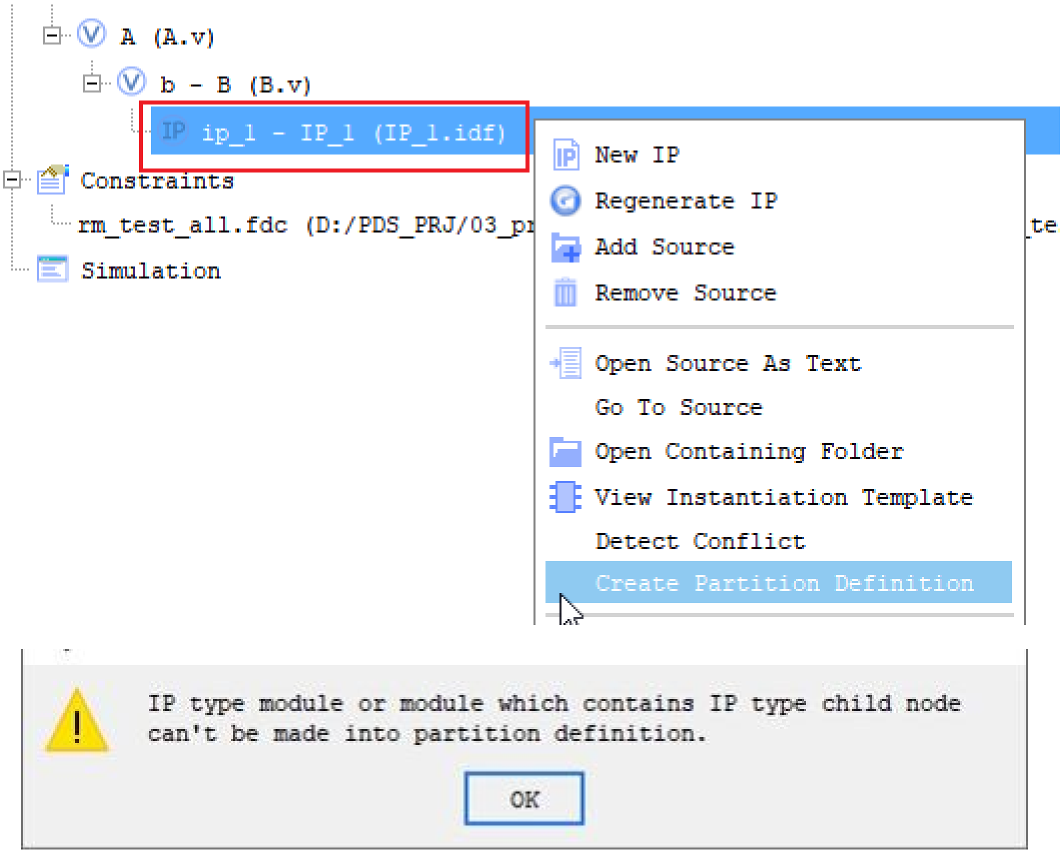


Figure 7-13 Do not operate 4

(6) A module whose child nodes contain PD instances cannot be created as a PD .

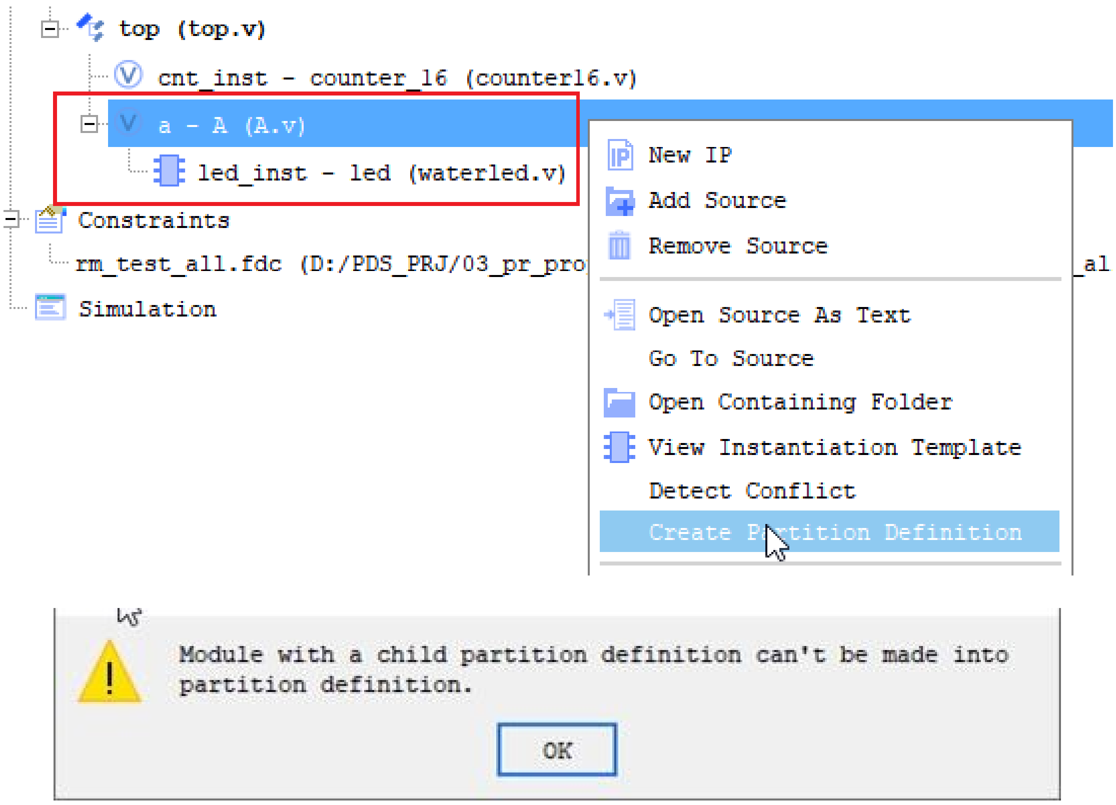


Figure 7-14 Do not operate 5

(7) If the parameter value passed when the Module is instantiated is not equal to the initial value of the corresponding parameter in the module definition, the module cannot be created as a PD .

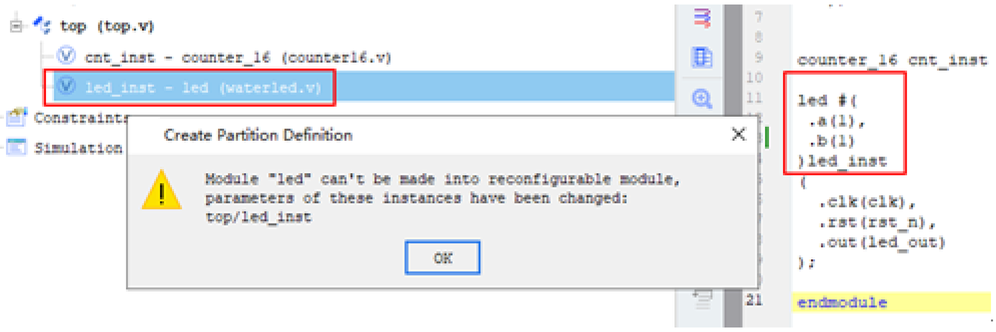


Figure 7-15 Do not operate 6

(8) When creating a PD for a Module , if a module under the module level is instantiated in other levels, the PD cannot be created .

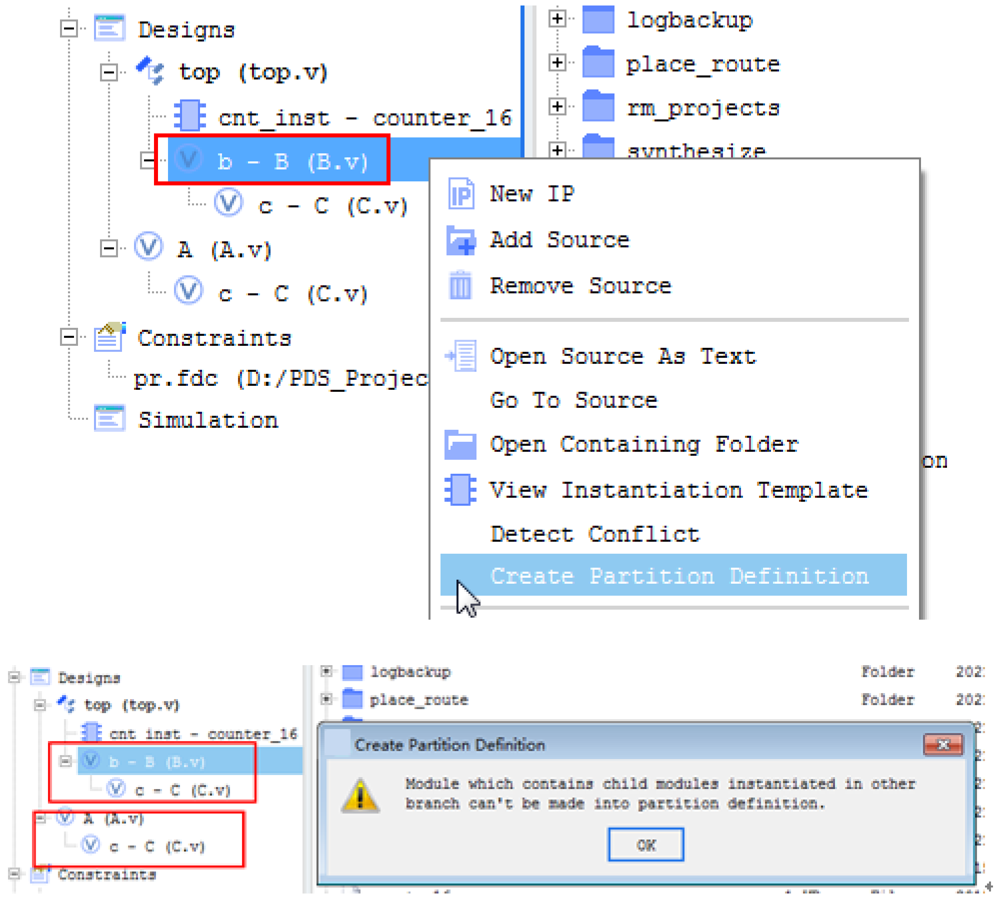


Figure 7-16 Do not operate 7

7.2.8 View and edit PD properties

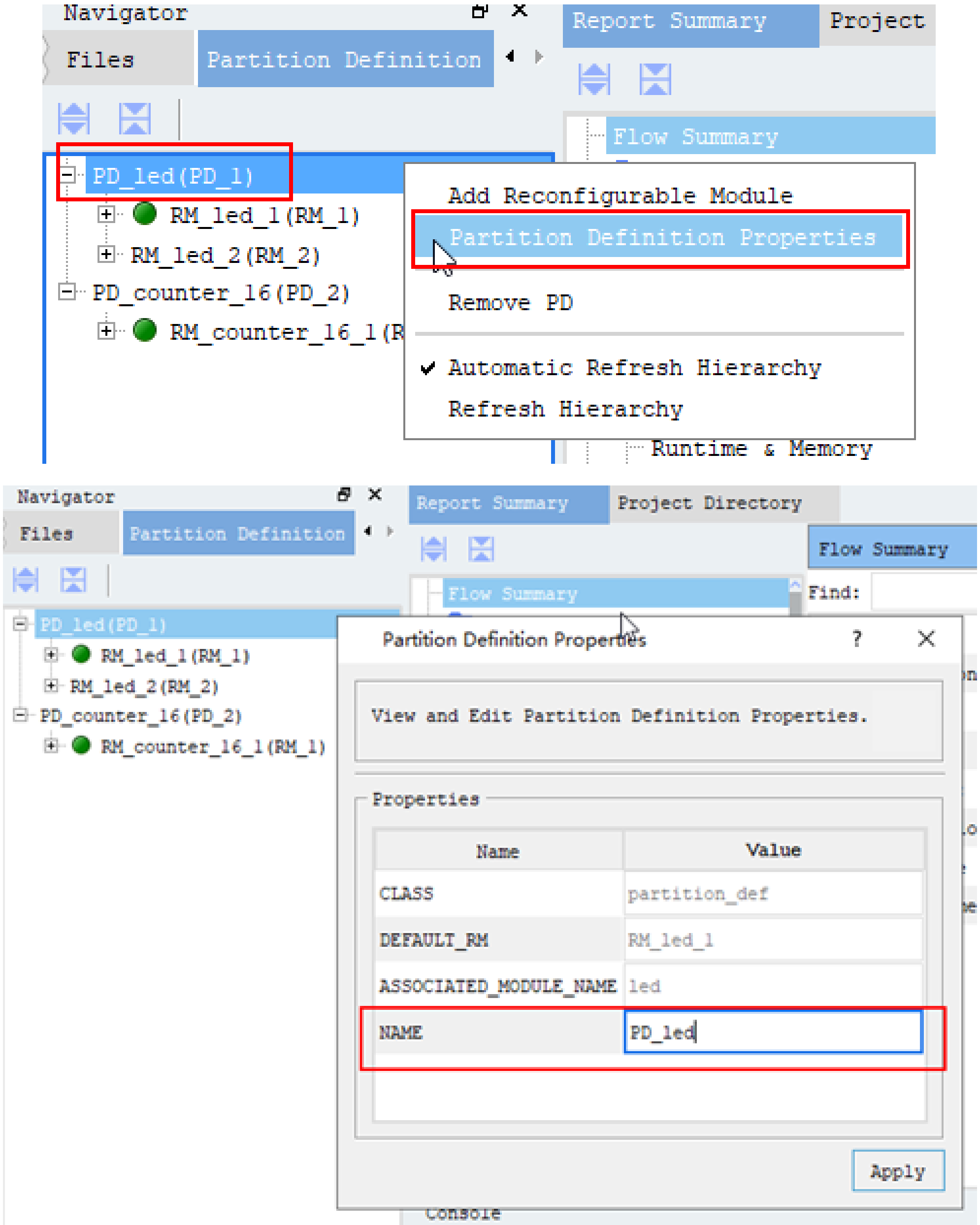


Figure 7-17 View and edit PD attribute operations

7.3 Delete Partition Definition

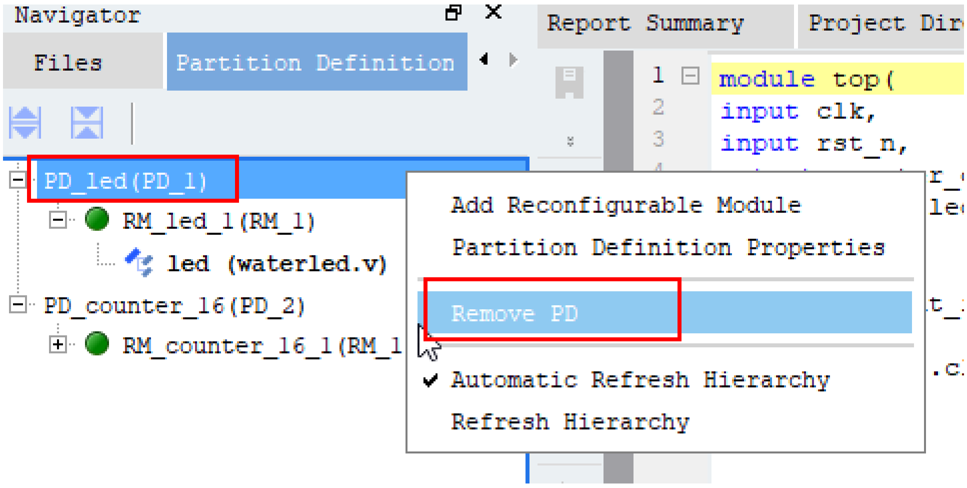


Figure 7-18 remove PD

The interface before deletion is as shown in the figure below:

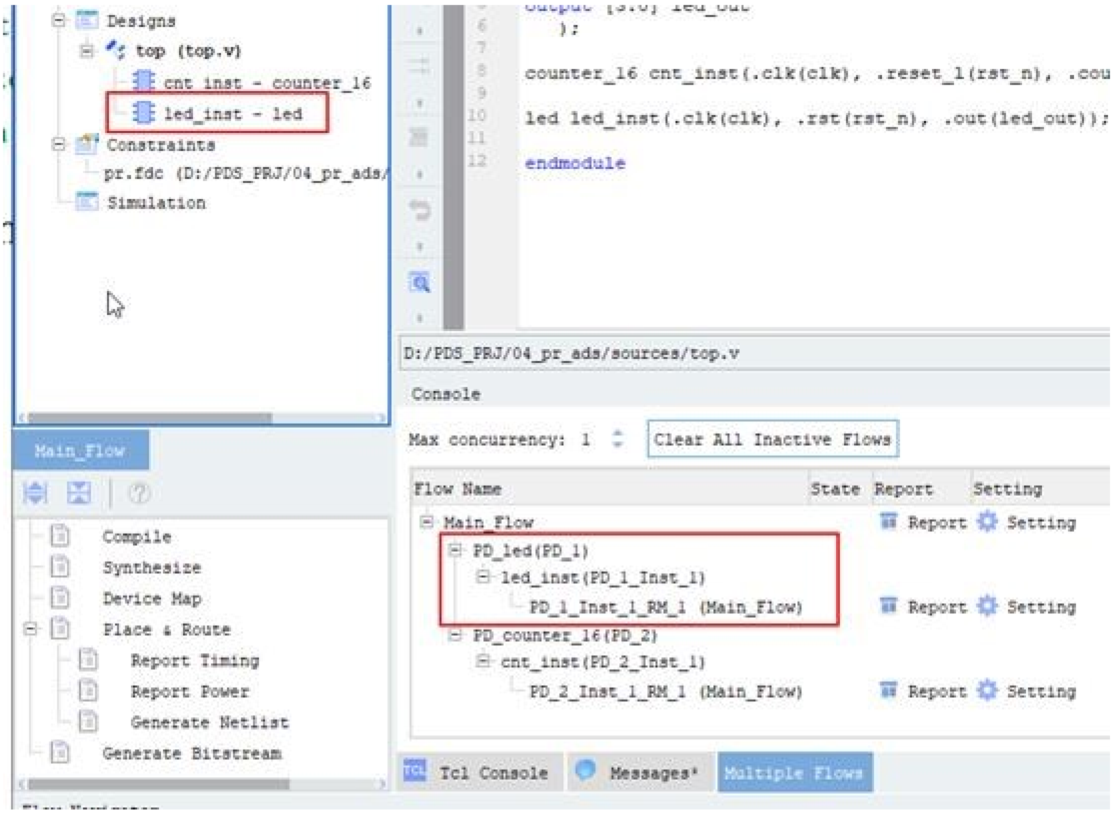


Figure 7-19 delete the front interface

The interface after deletion is as shown in the figure below

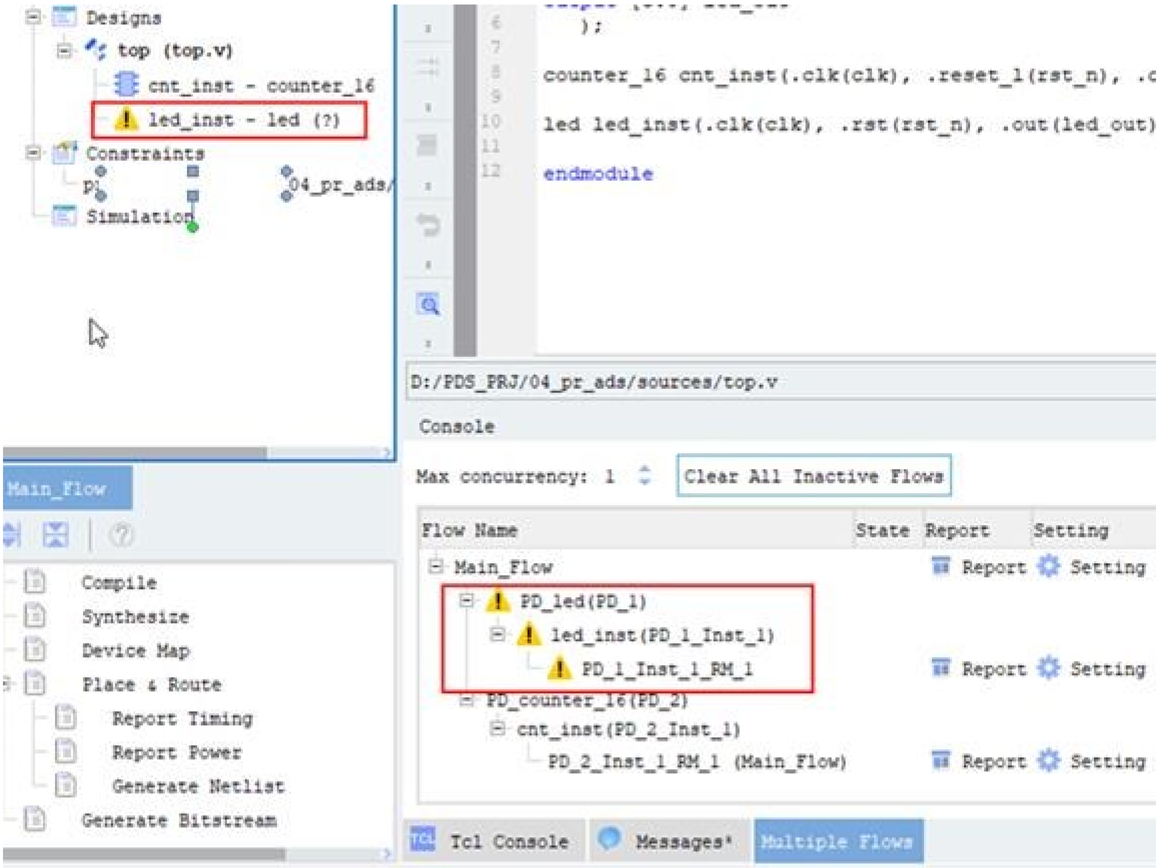


Figure 7-20 interface after deletion

The " ! " icon here indicates that the PD_Inst or RM or PD corresponding to RM_Flow does not exist.

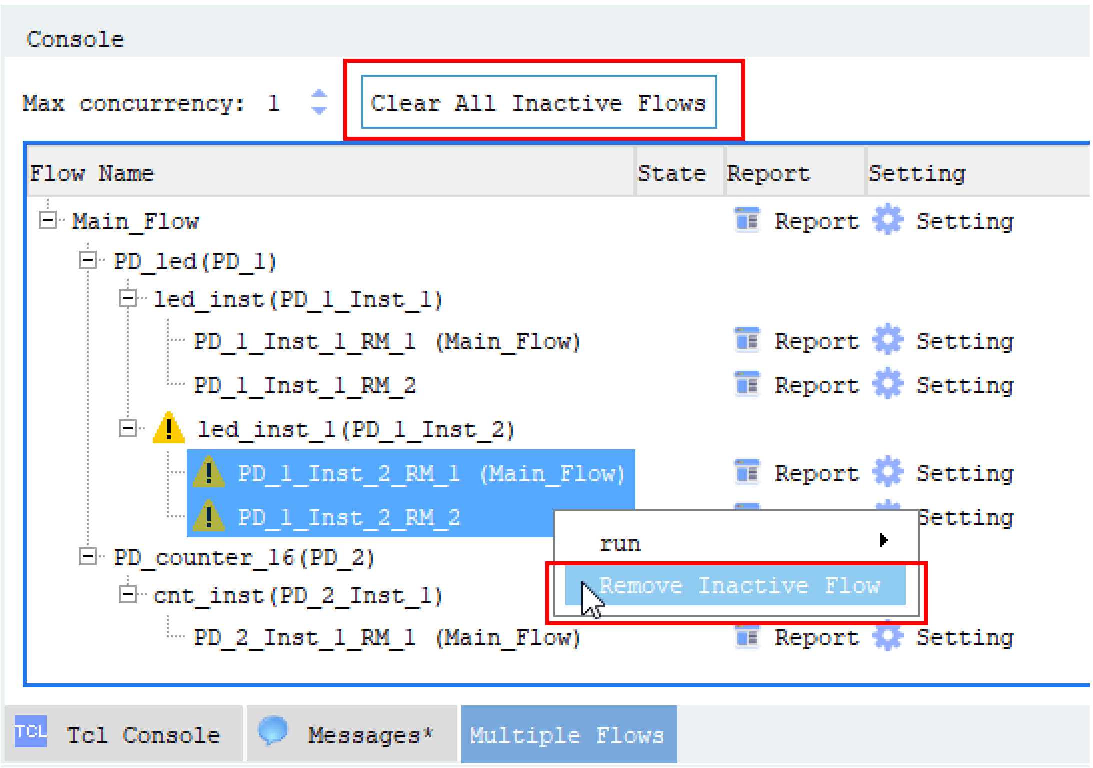


Figure 7-21 Remove inactive flow

Inactive Flow can be deleted through the above two operation interfaces .

Note: Because the corresponding design files are deleted from the main project and added to the PD 's default RM management when creating a PD , so after deleting the PD , the project does not have the design files of the PD 's default RM management , and the user needs to re-add these design files to main project.

In future, the function of deleting PD will be optimized. When the user deletes PD , the user will be prompted to select the design file to restore to the main project.

7.4 Add Reconfigure Module

7.4.1 Operation demonstration

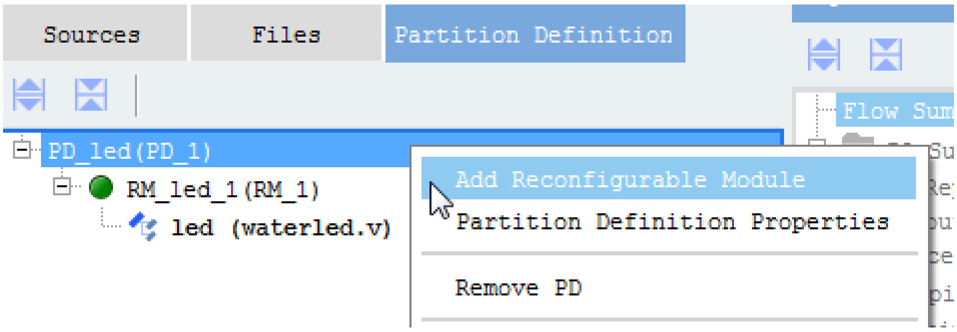


Figure 7-22 Add RM

Right-click the corresponding PD and select " Add Reconfigurable Module ".

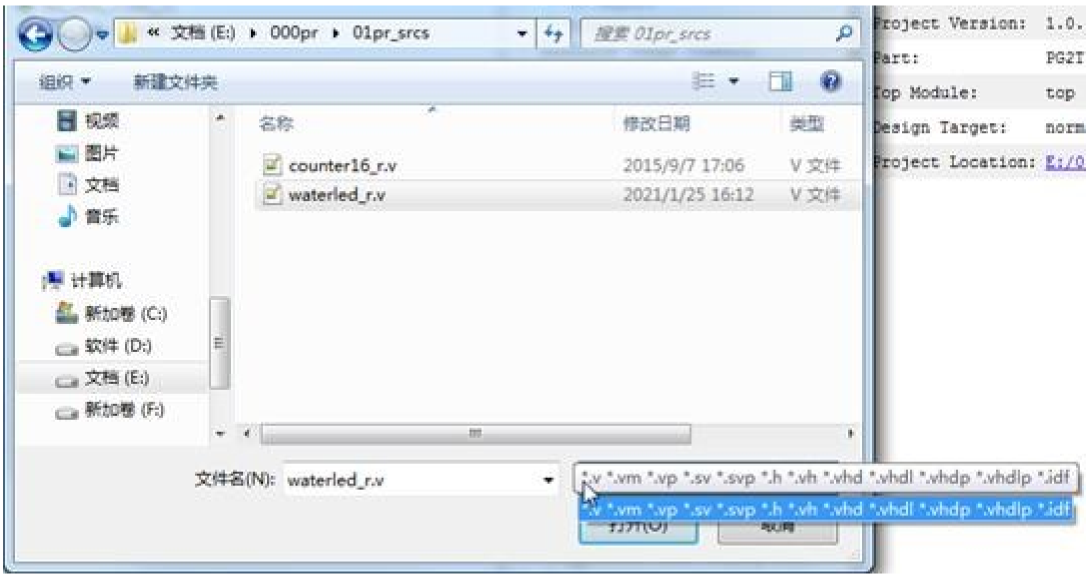


Figure 7-23 Add page

Select the design file that needs to be added to RM .

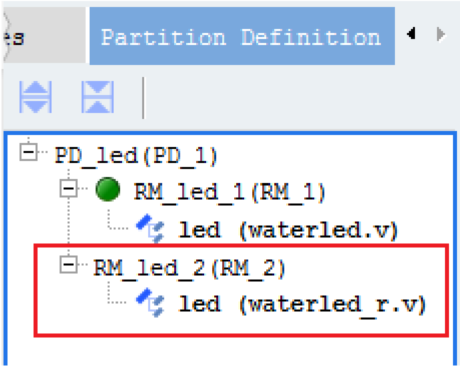


Figure 7-24 after adding RM

7.4.2 View and change RM properties

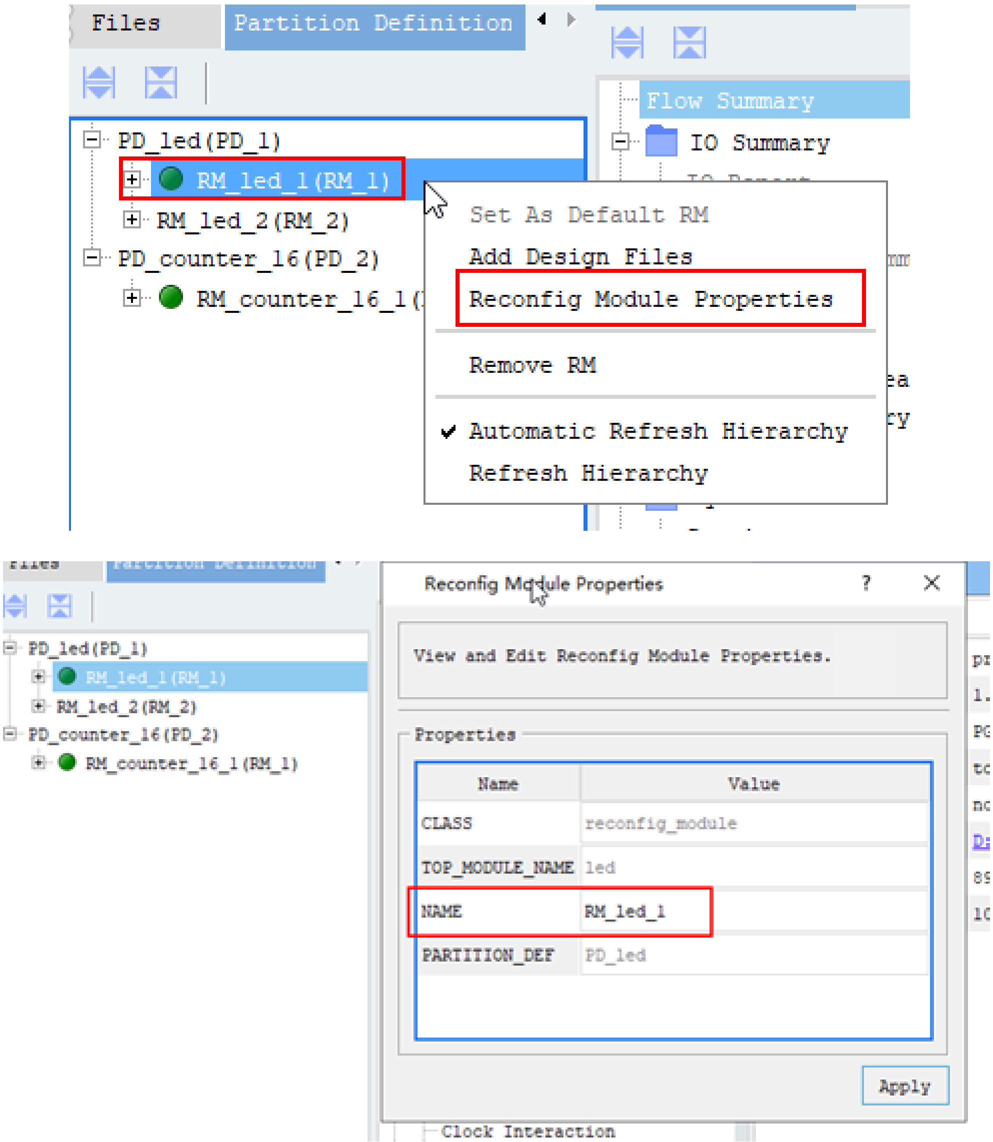


Figure 7-25 View and change RM

7.5 Delete Reconfigure Module

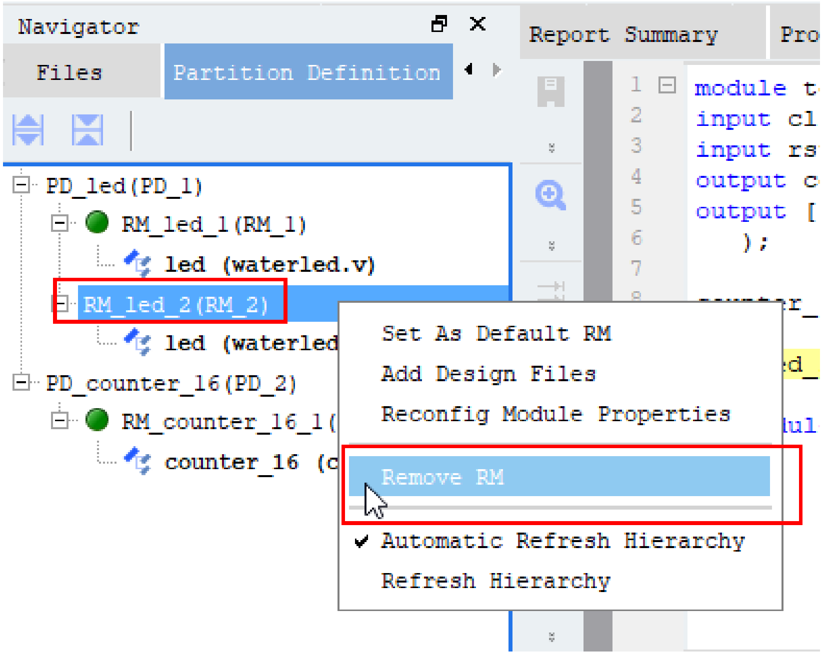


Figure 7-26 Delete RM

The interface before deletion is shown in the figure below

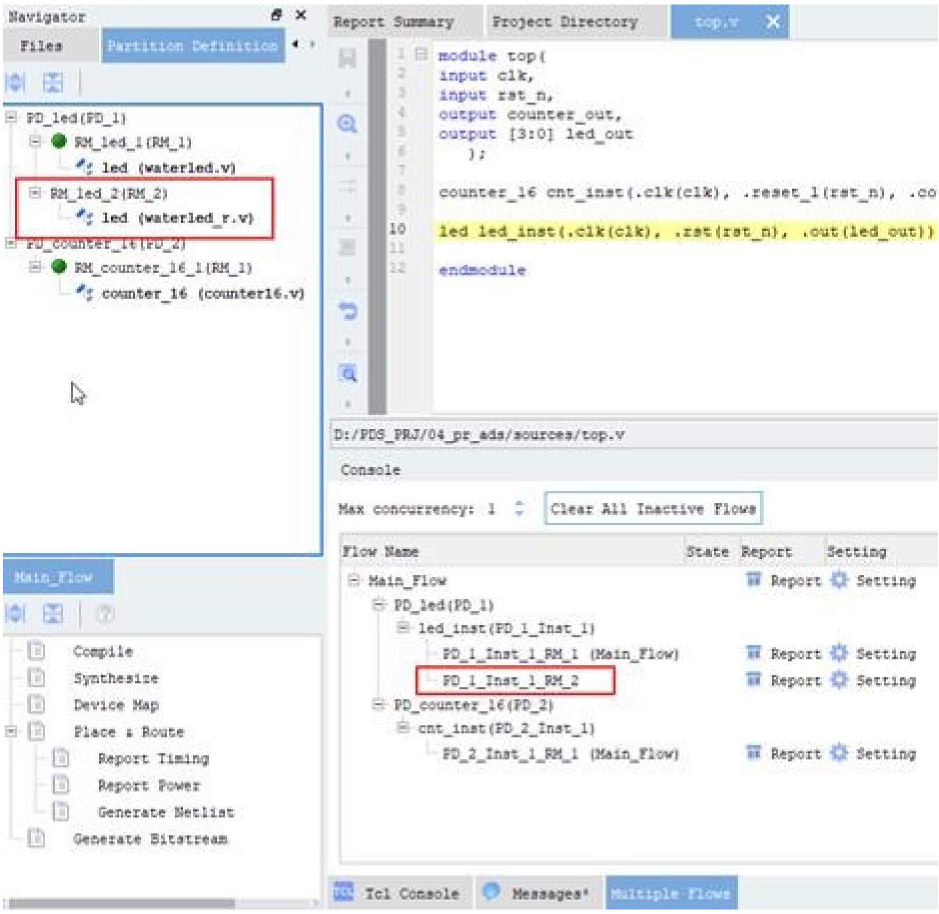


Figure 7-27 Delete RM ex

The interface after deletion is as shown in the figure below

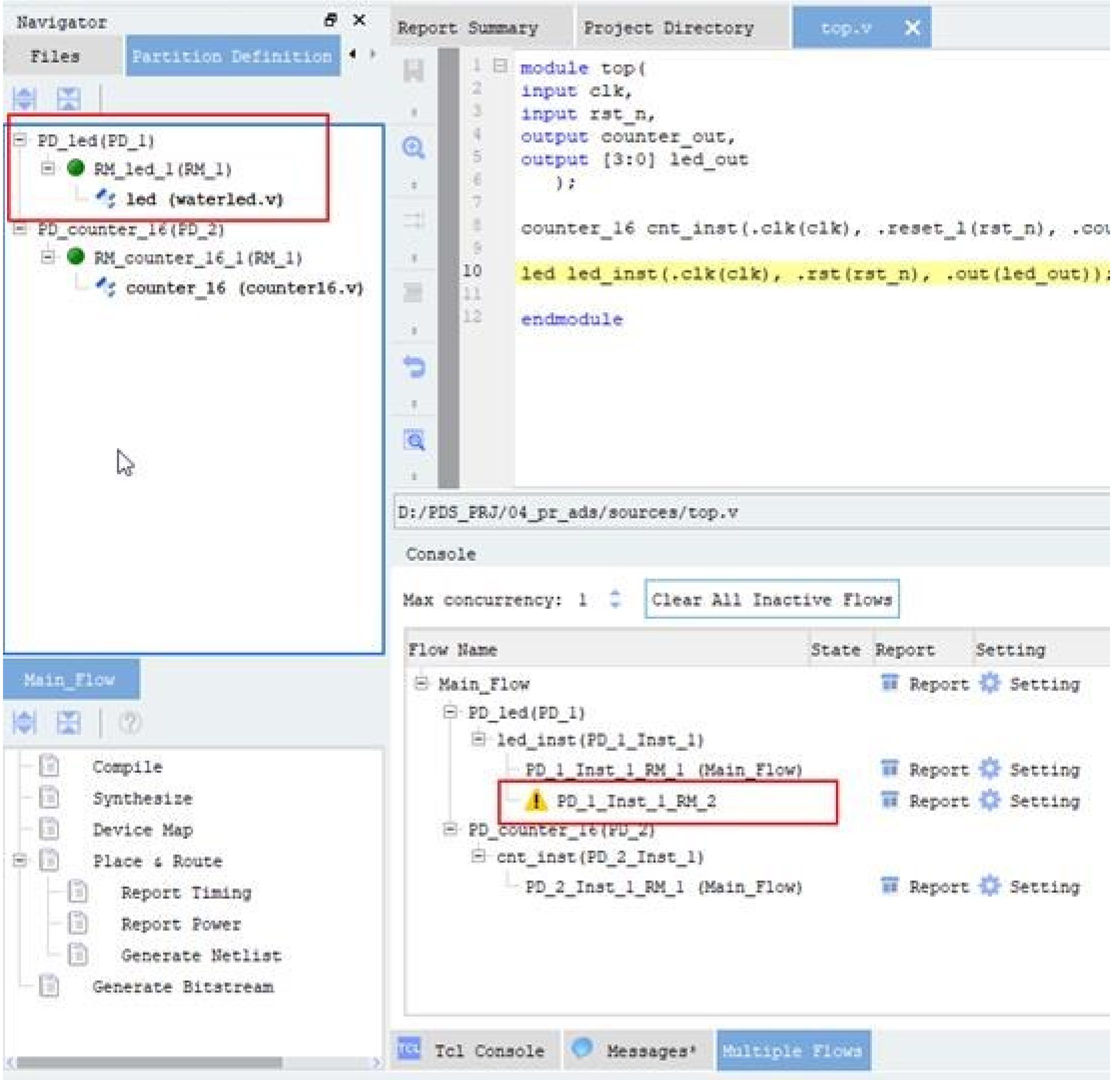


Figure 7-28 After removing RM

The " ! " icon here indicates that the PD_Inst or RM or PD corresponding to RM_Flow does not exist.

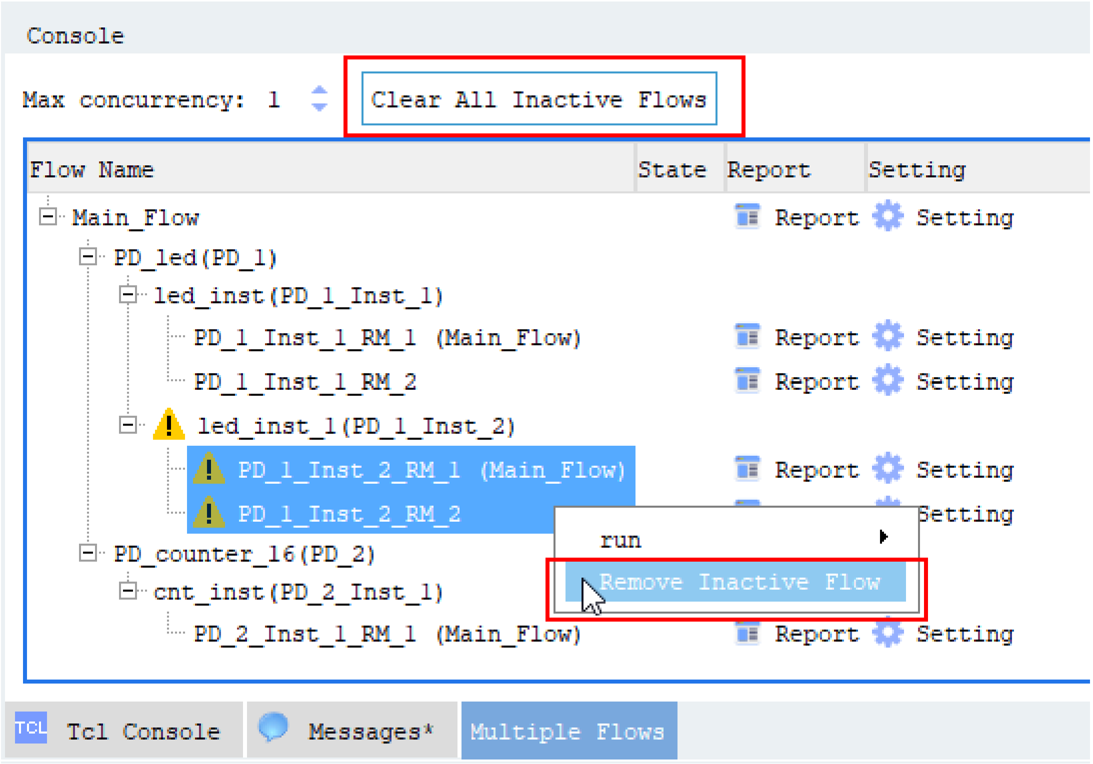


Figure 7-29 Delete IF

Inactive Flow can be deleted through the above two operation interfaces .

7.6 RM adds and deletes Design files

7.6.1 RM adds Design file

Right click on RM to add Design file

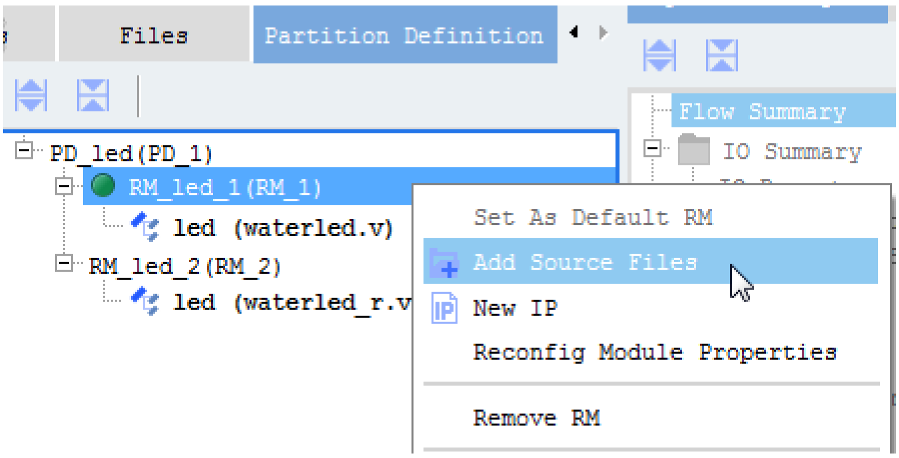


Figure 7-30 RM Add Design

Right-click on the Module Hierarchy node of RM to add the Design file

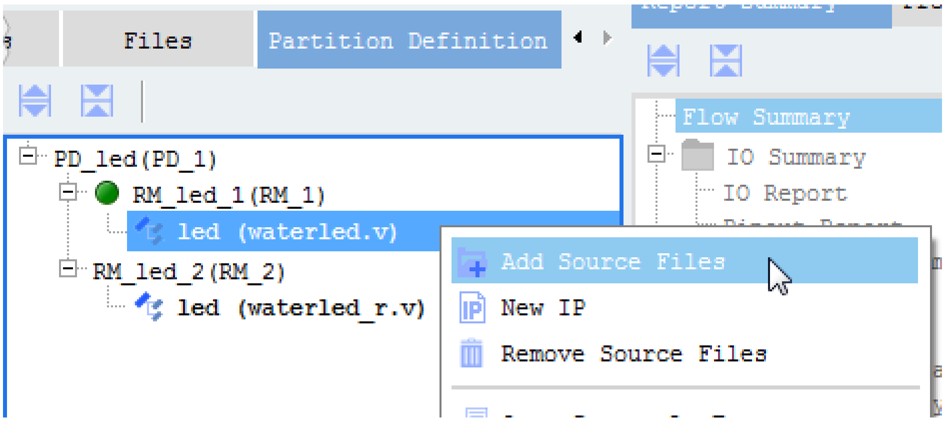


Figure 7-31 Add Design to the module heir node of RM

7.6.2 RM 's Top Module

Currently, the interface of the top module of each RM of the same PD must be consistent with the interface of the default RM of the PD (that is , RM1 of the PD), including the port number, type, sequence and name of the module .

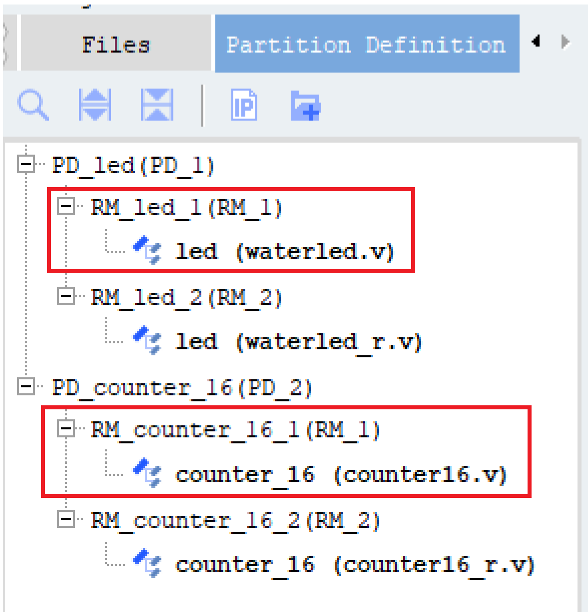


Figure 7-32 RM 's top module

For example, the interface of the top module of RM_led_1 (PD_1_RM_1) is as follows

led(input clk, input rst, output out);

Then the interface of the top module of RM_led_2 (PD_1_RM_2) should be completely consistent with the above interface.

For example, the interface of the top module of RM_counter_16_1 (PD_2_RM_1) is as follows

module counter_16(input clk, input reset, output reg[3:0] counter);

Then the interface of the top module of RM_counter_16_2 (PD_2_RM_2) should be completely consistent with the above interface.

7.6.3 RM delete Design file

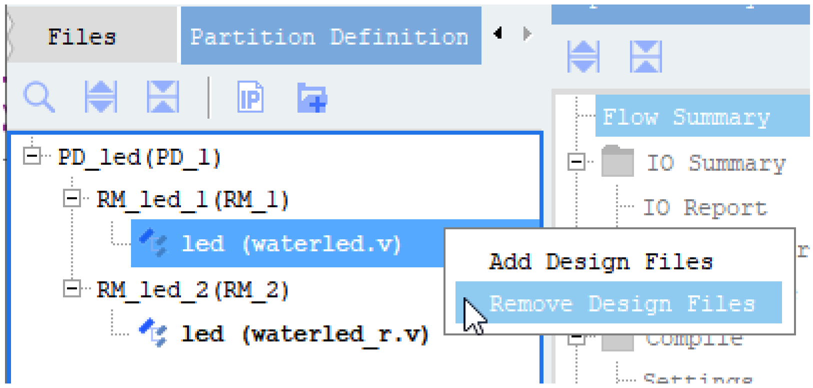


Figure 7-33 RM Delete Design

7.7 Add / Remove PD_Instance

7.7.1 Add PD_Instance

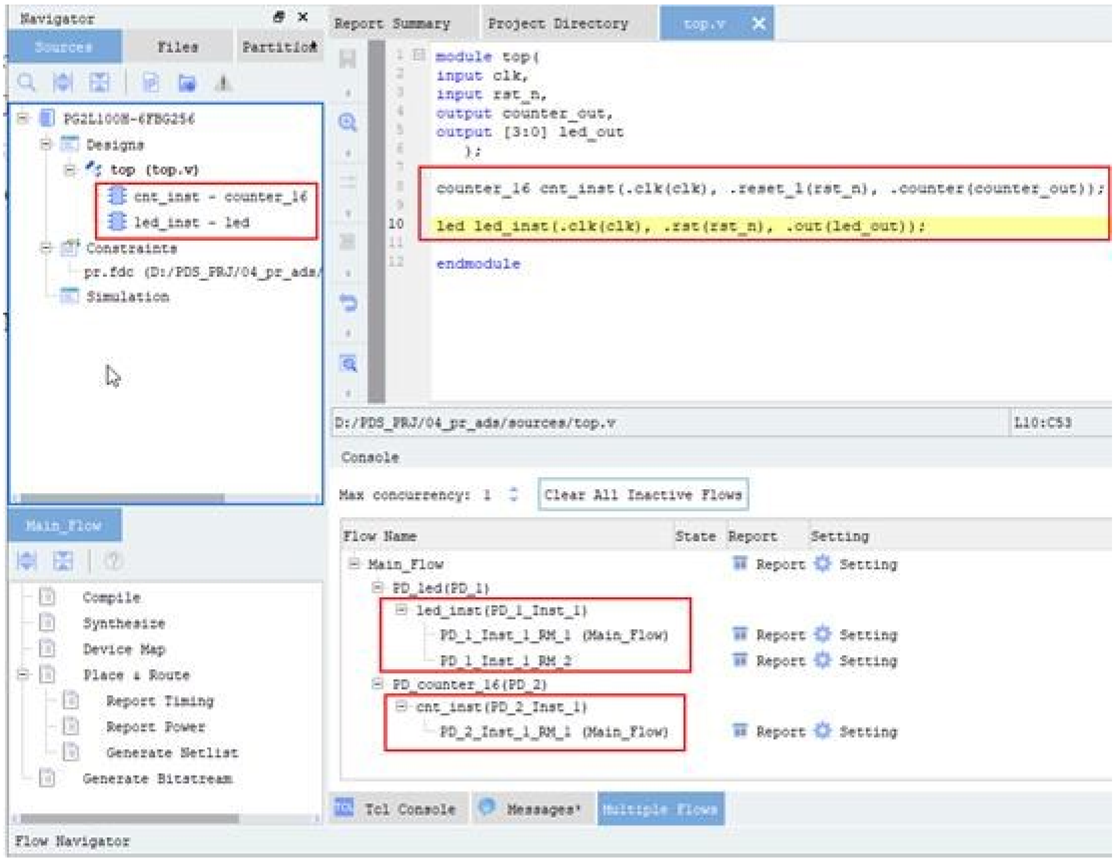


Figure 7-34 Original design and interface

The original design and interface are as shown in the figure above, after modifying the design file and adding a pd_inst , the design and interface are as shown in the figure below

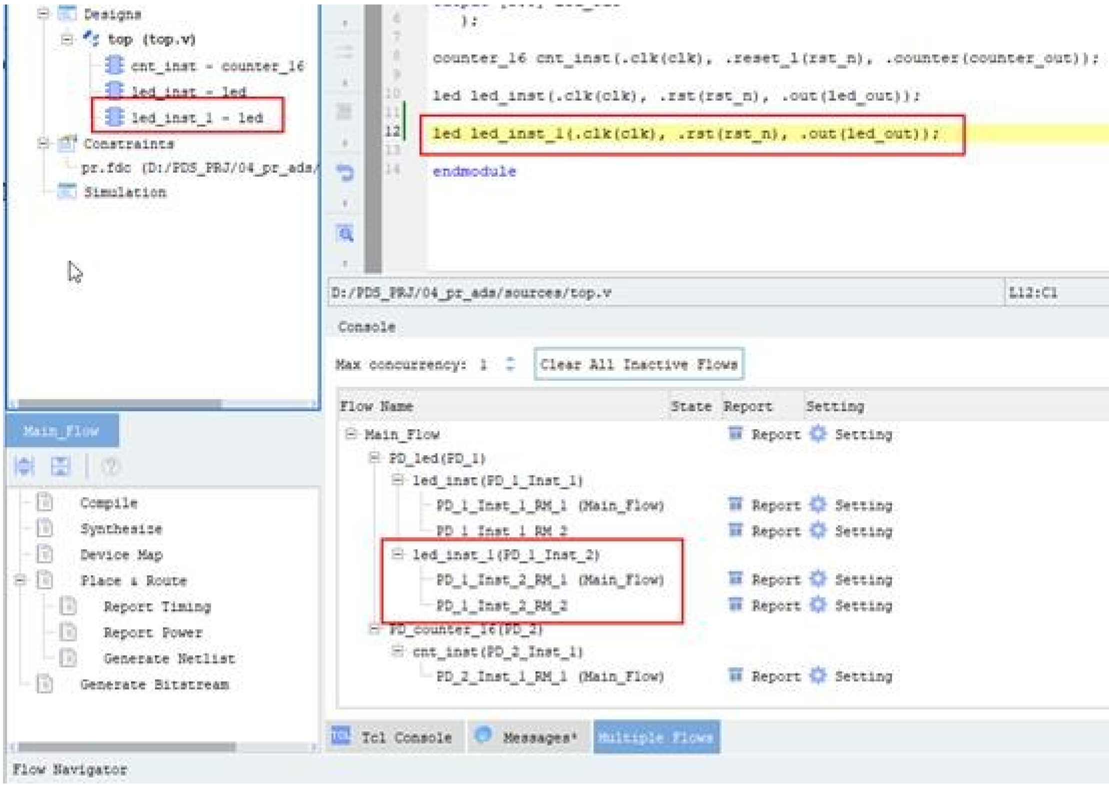


Figure 7-35 after adding

7.7.2 Delete PD_Instance

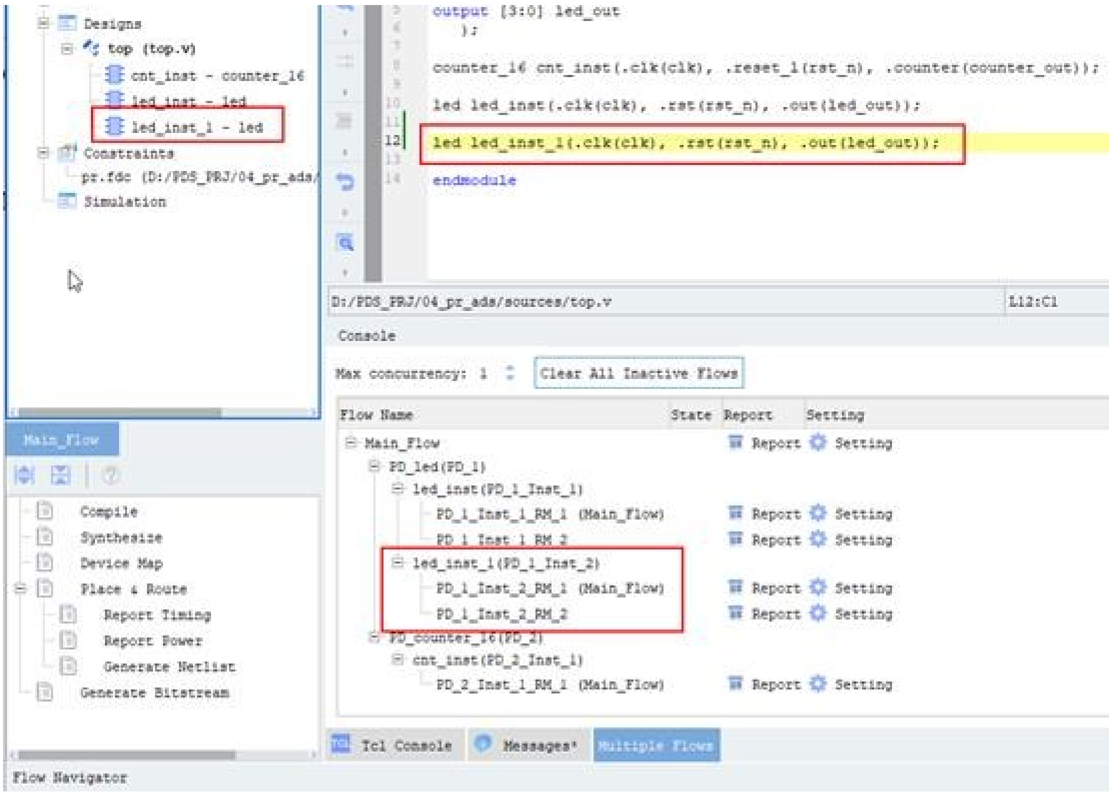


Figure 7-36 Original design and interface

The original design and interface are shown in the figure above, after modifying the design file and deleting a pd_inst , the design and interface are shown in the figure below

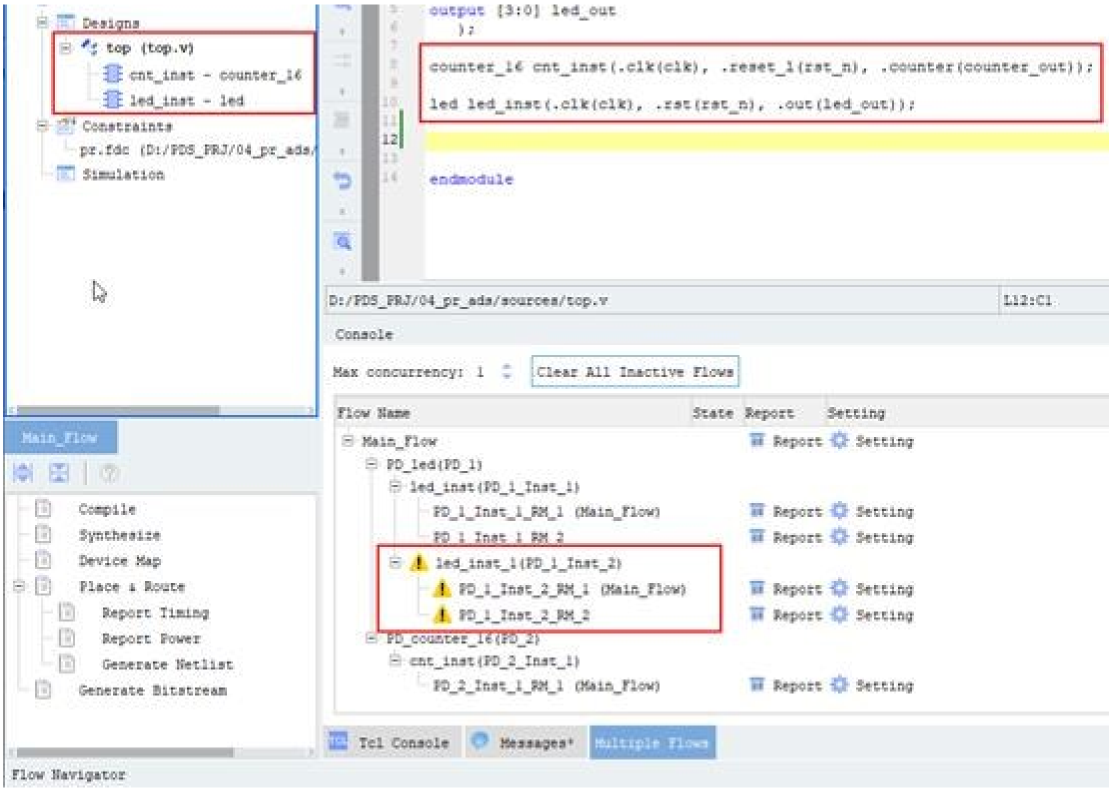


Figure 7-37 after deletion

The " ! " icon here indicates that the PD_Inst or RM or PD corresponding to RM_Flow does not exist.

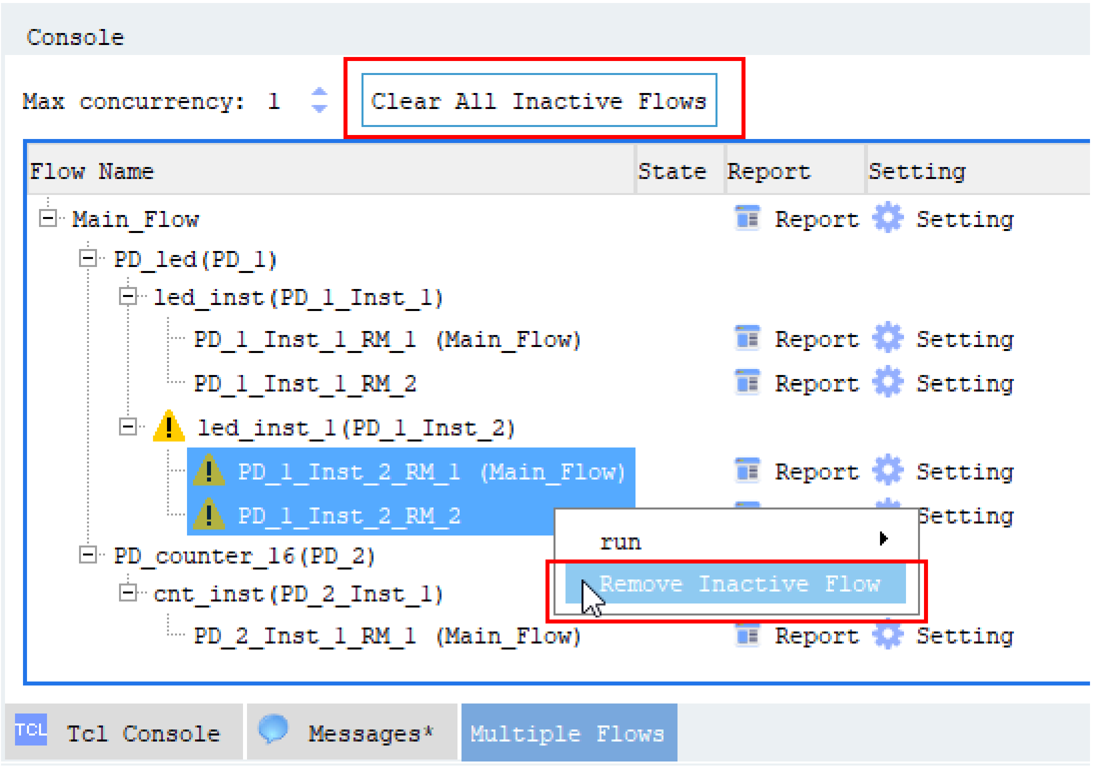


Figure 7-38 Delete Inactive Flow

Inactive Flow can be deleted through the above two operation interfaces .

7.8 Constrained reconfigurable region

At present, the physical constraints on the dynamic area can be completed in UCE as follows:

(1) Draw a region (region1) in UCE , and the drawing method is consistent with the region constrained by the drawing region. details as follows:

Click the Region Mode button to enter the regional mode. Right-click the menu Draw Region on the Floorplan , at this time the mouse becomes a cross shape, press and hold the mouse, and draw an area on the FloorPlan . After the mouse is released, click the button OK in the pop-up window "new region" , that is, the region region1 is successfully created.

(2) Constrain the active RM Instance (rm_inst) to the region (region1) drawn in step 1. The method is the same as constraining the Instance to the region. details as follows:

Click the Design Browser button of UCE (the shape is the letter N) , select rm_inst in the Design Browser , and drag the Instance to region1 .

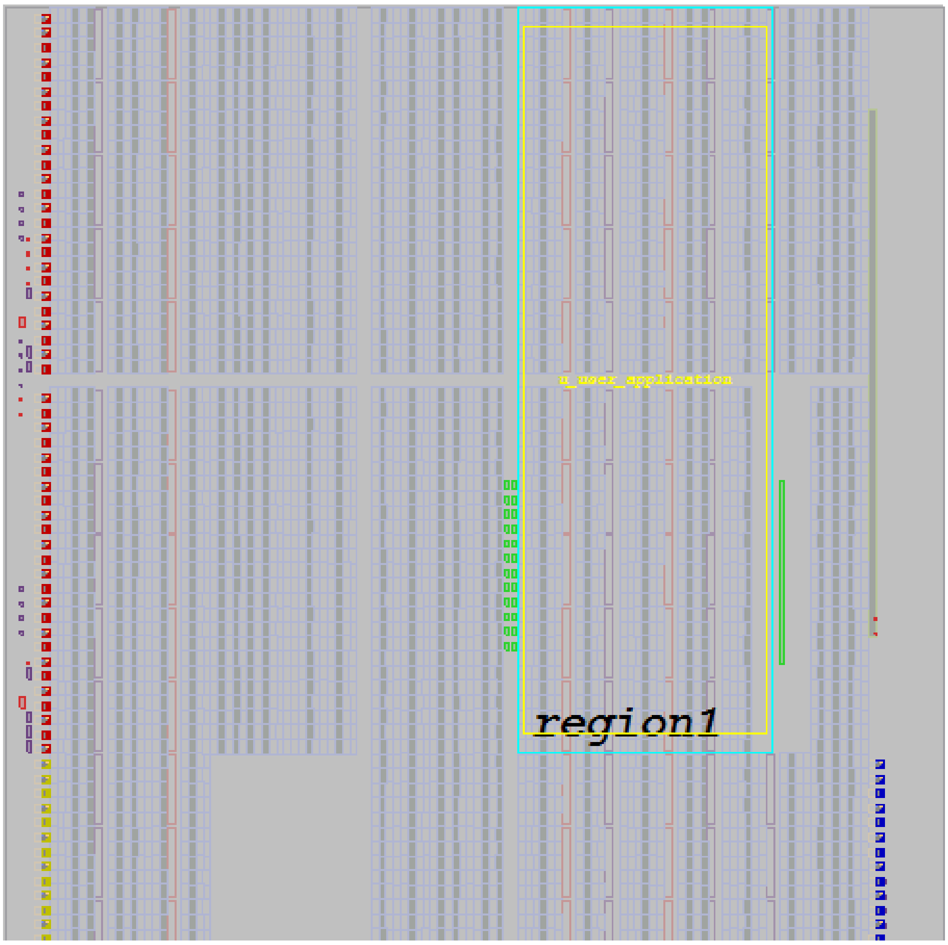


Figure 7-39 region1

(3) Add the PAP_EXCLUSIVE_REGION attribute to region1 , indicating that region1 is a dynamic region, and the software will expand the dynamic region drawn by the user according to certain rules.

The specific operation is: click Region on the Floorplan , Set Exclusive Region and Unset Exclusive Region in the right-click menu , corresponding to setting the attribute Exclusive region and canceling the attribute Exclusive region of the region respectively . After setting this property, the Region style is a dense solid-grain shadow type, and the range is highly densely covered by white particles. The name of the Region is displayed in bold below , and the mark " RM :" in front of the Region indicates that this attribute is used for local dynamic reconfiguration.

add the PAP_EXCLUSIVE_REGION attribute in fdc , you need to declare the Region first and then set the attribute for the Region , namely:

define_global_attribute {PAP_REGION} {region1(21,24,42,43);}

define_global_attribute {PAP_EXCLUSIVE_REGION} {region1}

(4) Not all resources on the chip can be reconfigured, so not all resources can be divided into reconfigurable areas. The leftmost two columns and the rightmost two columns of SRBs of the chip and all resources in the tiles where these SRBs are located , global clock resources, and all resources in the SRB tiles that use the same frame bit stream as these resources cannot be divided into reconfigurable areas . By avoiding the above-mentioned resources, it is possible to obtain the X- direction coordinate range of the resources that are allowed to be allocated to the reconfigurable area in the UCE when the constraints are configured. The range of PG2L100H is [6, 63], [68, 111], .

In addition, CCS , ADC , PCIE , and the resources in the tile where the SRB near the above three resources cannot be divided into the reconfigurable area, that is , [26, 47, 50, 149], [96, 114, 150, 199] cannot be divided into reconfigurable regions. The coordinate format above is [x1, x2, y1, y2] , and all the above coordinates are floor plan coordinates, and all intervals are closed intervals.

Constraints are adaptive. If the illegal area is included, the software will perform adaptive cutting according to the Y axis, and the reconfigurable range may be reduced. If it cannot be cut into an area, a prompt will be given. At the same time, it will be adapted to the upper and lower boundaries of the clock domain, and the reconfigurable range may be expanded.

7.9 Run Flows

7.9.1 Correspondence between process and PD , PD Instance and RM

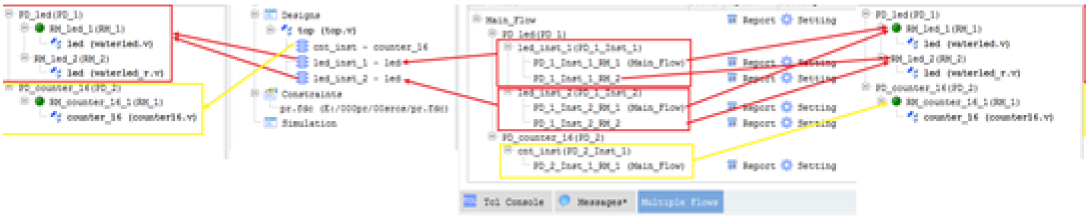


Figure 7-40 Correspondence between process and PD , PD Instance and RM

In the figure above, PD_led (PD_1) has 2 Instances : led_inst_1 and led_inst_2 ; PD_counter_16 (PD_2) has 1 Instance : cnt_inst .

PD_led (PD_1) manages 2 RMs : RM_led_1 (PD_1_RM_1) and RM_led_2 (PD_2_RM_2); PD_counter (PD_2) manages 1 RM : RM_counter_16_1 (PD_2_RM_1) .

the " Multiple Flows " component, there are two nodes led_inst_1 and led_inst_2 under the PD_led(PD_1) node, which means that PD_led (PD_1) has two Instances : led_inst_1 and led_inst_2 . There are 2 Flow nodes under the led_inst_1 node: PD_1_Inst_1_RM_1 and PD_1_Inst_1_RM_2 ; PD_1_Inst_1_RM_1 means that led_inst_1 uses PD_1_RM_1 to run the process, and PD_1_Inst_1_RM_2 means that led_inst_2 uses PD_1_RM2 to run the process.

7.9.2 Switch process tree

in the " Multiple Flows " part, and the left side will switch to the corresponding process tree. You can use the process trees " Run ", " Rerun " and " Rerun All ".

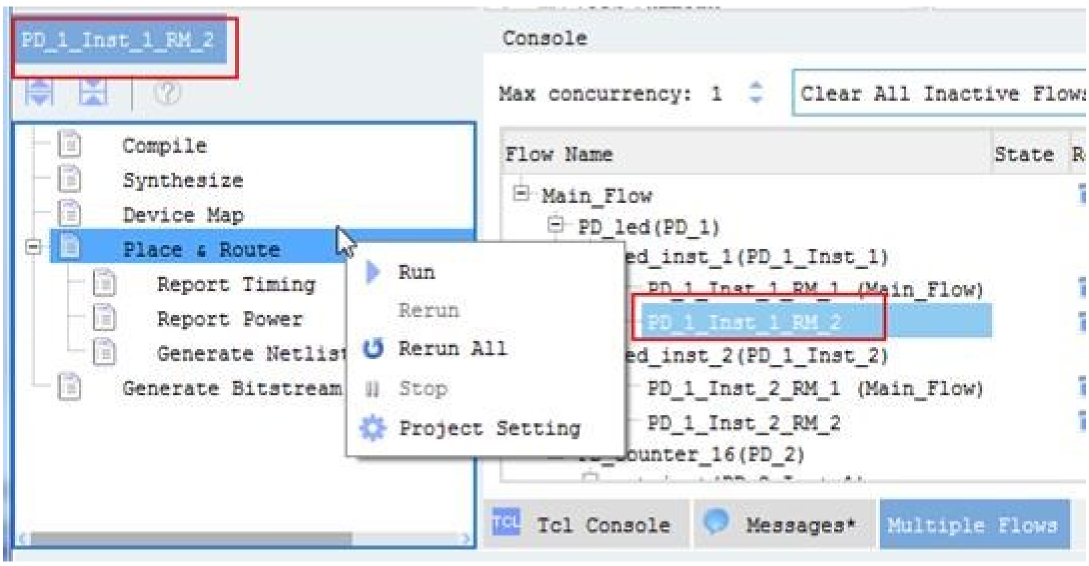


Figure 7-41 switch process tree

7.9.3 Process dependency

The " Synthesize " of the RM process depends on the " Report Timing " of the main process, that is, before running the " Synthesize " of the RM process, the main process will be automatically run to " Report Timing ".

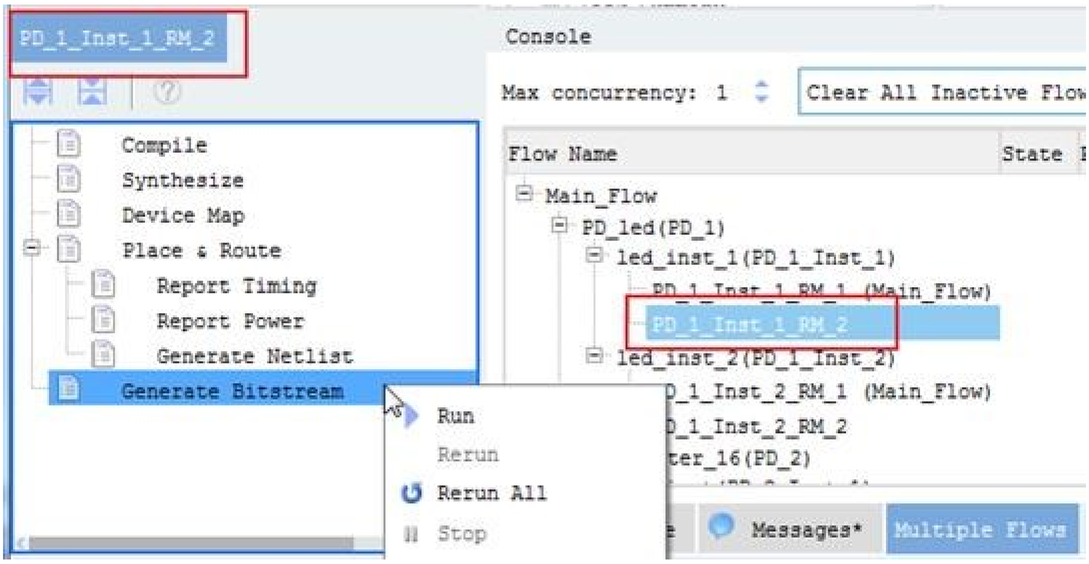


Figure 7-42 Process dependencies

For example, to run the " Generate Bitstream " of the " PD_1_Inst_1_RM_2 " process in the above figure , before running Synthesize , it will automatically run " Main Flow " to " Report Timing ".

7.9.4 Process relationship

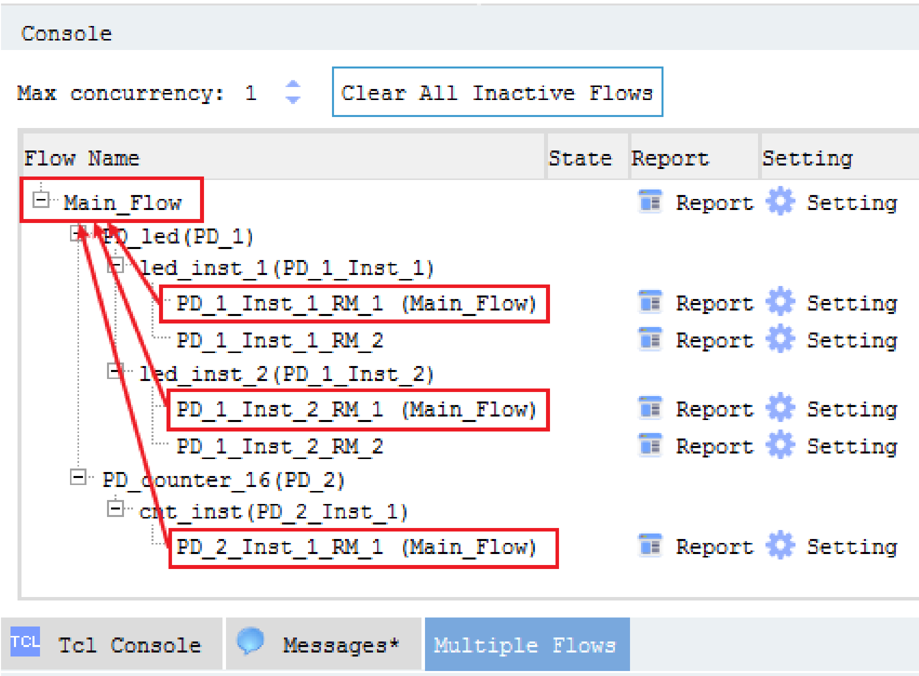


Figure 7-43 Process relationship

As shown in the figure above, the three processes of PD_1_Inst_1_RM_1 , PD_1_Inst_2_RM_1 and PD_2_Inst_1_RM_1 are essentially Main Flow , and running these processes means running the main flow. Because when running the main process, the RM_1 of the PD will be configured to each Instance of the PD to run.

7.9.5 Processes run in parallel

If there is no dependency between the processes or the process dependency conditions are satisfied, the processes can run in parallel.

There is no dependency between all reconfiguration processes, so the reconfiguration processes can run in parallel.

Synthesize of the reconfiguration process depends on the Report Timing of the main process, so the Compile of the main process and the reconfiguration process can run in parallel. When the reconfiguration process needs to run Synthesize, the reconfiguration process will wait for the main process to finish running Report Timing . The Synthesize and subsequent steps of the configuration process can run in parallel with the steps after the Report Timing of the main process (the Generate Bitstream of the reconfiguration process depends on the Generate Bitstream of the main process, so these two steps cannot be run in parallel).

This means that when a process is running, other processes can still be started to run. As shown below:

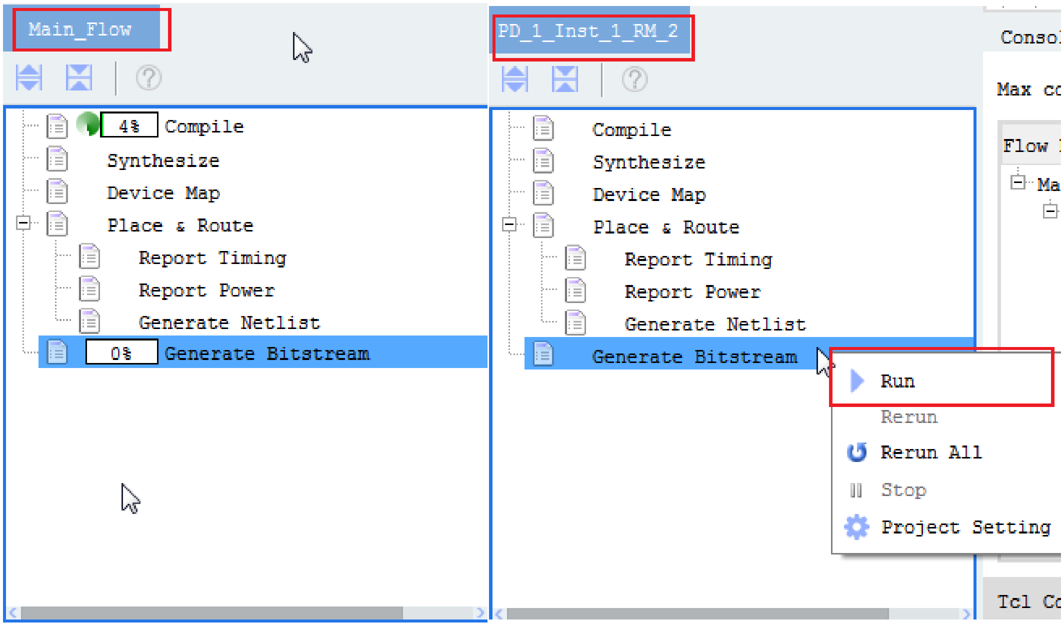


Figure 7-44 Running multiple processes

Or run multiple processes at the same time, as shown in the following figure:

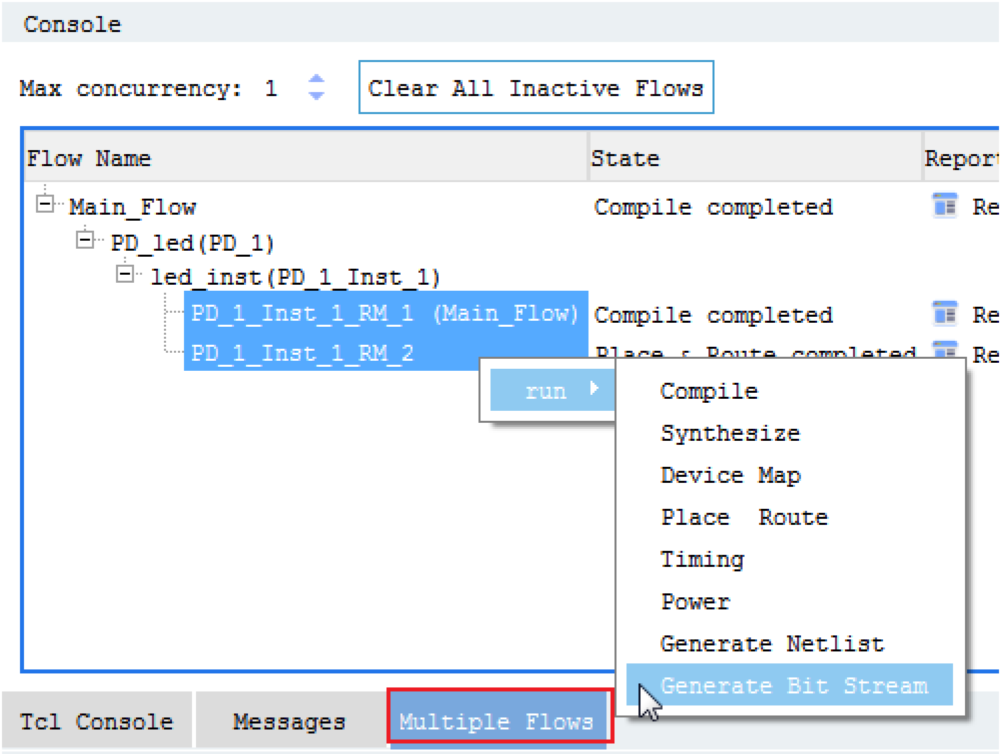


Figure 7-45 Start multiple processes at the same time

7.10 Component related

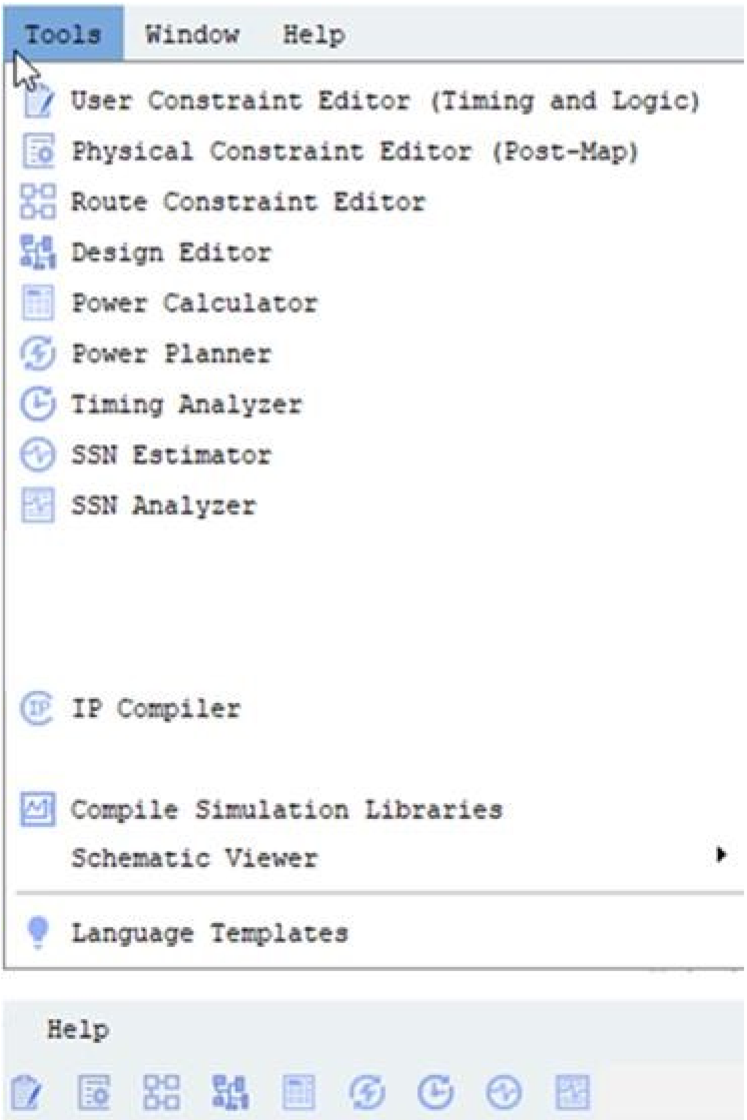


Figure 7-46 Main process support components

Only the main process supports the above components.

7.11 Project Setting

7.11.1 Operation demonstration

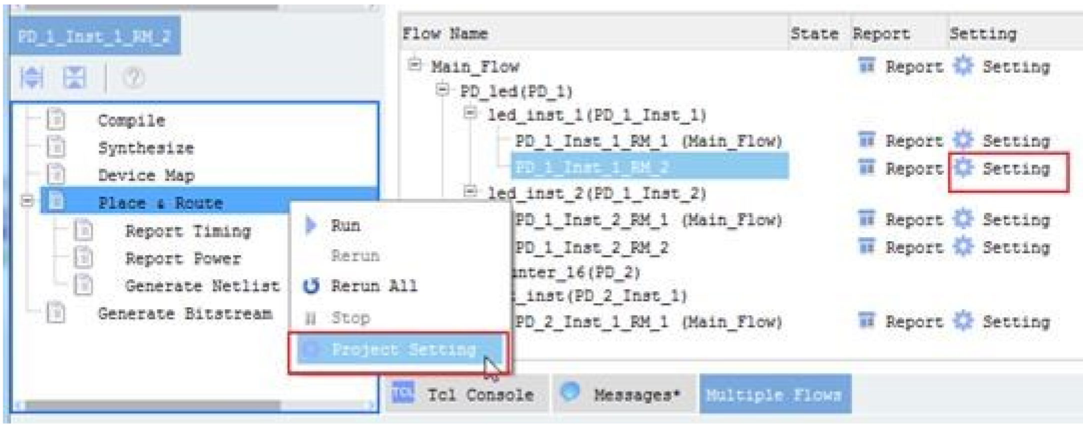


Figure 7-47 Open project setting

(1) Right-click on the process tree and select " Project Setting ".

(2) Click the "Setting" button of the corresponding process in the "Multiple Flows" component.

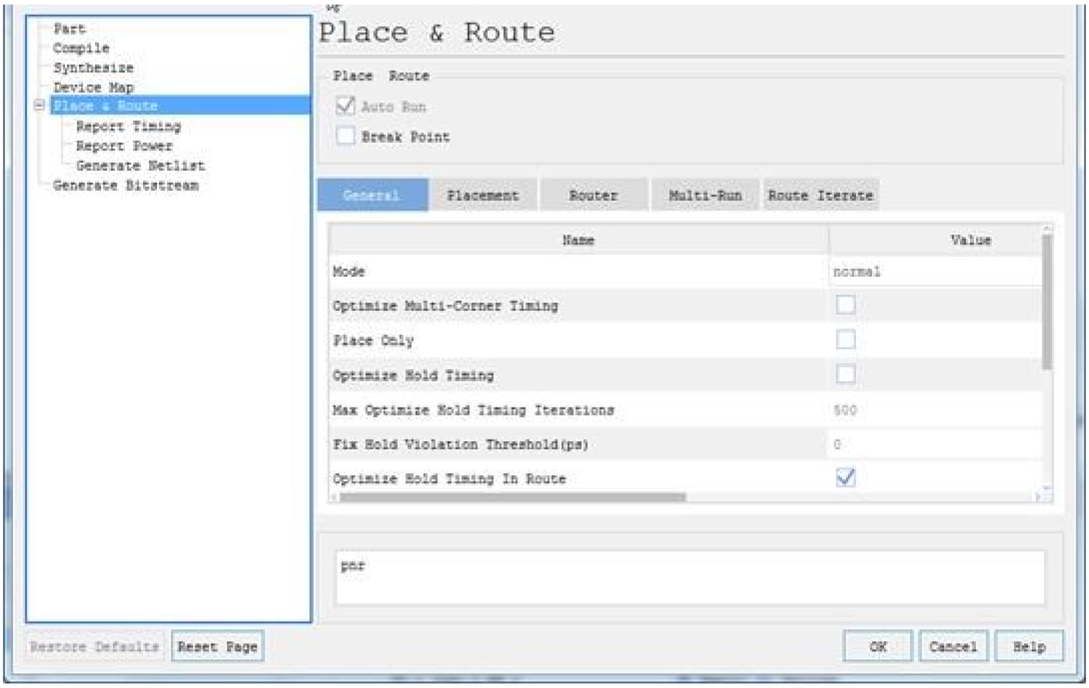


Figure 7-48 Project settings interface

7.11.2 Relevant instructions

(1) Each process has a corresponding " Project Setting ".

(2) Changing the device or synthesis tool settings of any process will synchronize the settings to all processes.

(3) The three processes of PD_1_Inst_1_RM_1 , PD_1_Inst_1_RM_2 and PD_2_Inst_1_RM_1 are essentially Main Flow , so the "Project Setting" of these three processes is the " Project Setting " of Main Flow .

(4) The RM process currently does not have a " Simulation " setting, but the Main Flow does.

7.12 Report Summary

7.12.1 Operation demonstration

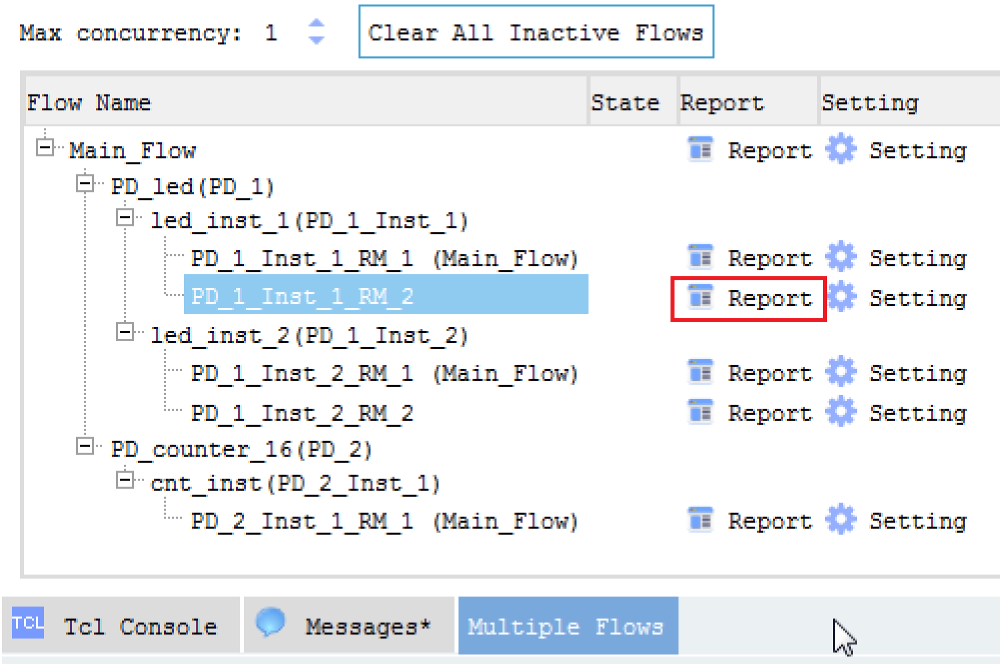


Figure 7-49 click report

Click " Report " of the corresponding process of " Multiple Flows ", and the " Report Summary " of the corresponding process will be displayed , as shown in the figure below.

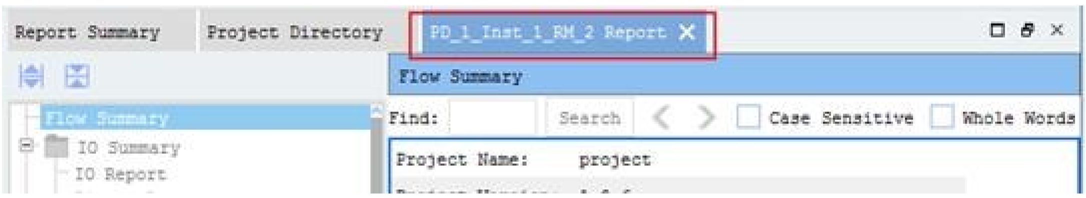


Figure 7-50 Report summary

7.13 Project files for the reconfiguration process

The project files of the reconfiguration process will be saved in the rm_projects folder of the project main directory. These project files are used to record the data of the reconfiguration process. When the project is opened, the data of the reconfiguration process can be read.

The reconfiguration project file is a part of the partial reconfiguration project; to enable the partial dynamic reconfiguration mode project, please open the main project file in the main project directory, and the reconfiguration project file in the rm_projects folder cannot be opened separately.

7.14 Bitstream Generation and Programming

7.14.1 bitstream file description

in both main flow and rm flow .

(1) Complete bit stream file: a file named after the design name , which contains data information of all areas (static and dynamic), can be programmed separately, and can actually observe the corresponding logic functions.

(2) Dynamic bit stream file: The file name is rm.sbit , which contains the functions corresponding to the dynamic logic and corresponds to the logical area divided by the dynamic area

(3) Static bit stream file: the file name is static.sbit , which contains all data except the data in the dynamic area.

When programming and downloading, the software configuration will automatically recognize rm.sbit and use dynamic reconfiguration for programming.

8 Software principles

8.1 File and Folder Naming Conventions

PDS suite folder naming rules: only alphanumeric underscore (_) bar (-) dot (.) @ and space ( ), but spaces cannot appear at the beginning or end of the pathname.

File Naming Rules: Only alphanumeric underscores (_) bars (-) dots (.) are allowed.

In particular, IPC file naming rules: only alphanumeric underscores (_) are allowed.

In the main interface of PDS and the dialog box of each component, when saving a file or filling in the path name, it will be judged according to this rule, and a prompt will be given if it does not meet the requirements .

8.2 Open Tool Software Rules in PDS Suite

PDS opens each tool software, one tool only opens one instance; when opening DE , only one DE can be opened .

When the tool software is open, you cannot create a project, close the project, save it as a project, or close the software; you need to close the relevant software before performing the corresponding operation (in this case, you will be prompted to close the tool software before proceeding).

When the input of each tool software is changed, the user shall be prompted to change accordingly, and the user shall be allowed to choose whether to reload the corresponding input.

8.3 The relationship between process and tool software

When the process is running, it is not allowed to open the tool software (the tool software that has already been opened will not be affected).

When the process is not running, it is allowed to open each tool software at the same time, and maintain its current process dependencies. For example, when opening PCE , dev_map and the previous steps must be completed first (if the process does not run to map when opening PCE , the process will first run to map , and then open PCE ; when opening DE , PnR and the previous steps must be completed first, and then open DE).

9 List of common commands

9.1 add_constraint specifies the constraint file

options	
-help	print help message
-copy	Copy the specified file to this project
parameter	
input_filename	specify an input filename

Table 9 -1 add_constraint

9.2 add_design specifies the design file

options	
-help	print help message
-library	Specifies the name of the logic library . The default is work
-define	define compile macros
-copy	Copy the specified file to this project
parameter	
input_filename	specify an input filename

Table 9-2 add_design

9.3 add_fic specifies the constraint file

options	
-help	print help message
-copy	Copy the specified file to this project
parameter	
input_filename	specify an input filename

Table 9 -3 add_fic

9.4 add_simulation specifies the simulation file

options	
-help	print help message

-library	Specifies the name of the logic library . The default is work
-define	define compile macros
-copy	Copy the specified file to this project
parameter	
input_filename	specify an input filename

Table 9-4 add_simulation

9.5 add_sources specified folder

options	
-help	print help message
-sub_directories	search subfolders
-copy	Copy the specified file to this project
-continue	Continue to add files when there is an error
-design	Specifies that the type of added file is a design file
-simulation	Specify the type of added file as a simulation file
-constraint	Specify the type of added file as a constraint file
-fic	Specify the type of added file as a core file
-ip	Specify the type of added file as IP file
-library	Specifies the name of the logic library . The default is work
-define	define compile macros
parameter	
input_dir	Specify a folder containing the input file, note : in tcl standard syntax, "\" is an escape character, you may need to change the " \ " in the windows folder path to " / " before running

Table 9 -5 add_sources

9.6 clean clear action state

options	
-help	print help message
-action	Specify an action name
-translate	Effective for report timing action
-configuration	Effective for report timing action

Table 9 -6 clean

9.7 set_arch specifies device information

options	
-help	print help message
-family	specify a family
-device	specify a device
-package	specify a package
-speedgrade	specify a speed class

Table 9-7 set_arch

9.8 compile Compile the user design

options	
-help	print help message
-top_module	Set the name of the top module
-include_path	Set the include path of the project

Table 9-8 compile

9.9 dev_map maps design to architecture

options	
-help	print help message
-packing_io	Set the name of the top module
-detail	Set the include path of the project
-generate_inferred_clocks	After checking, the clock will be inserted into the design that meets the conditions
-fanout	Only print Net or port objects with fanout greater than this value in the report
-fanout_number	The upper limit of the number of Nets whose number of fanouts printed in the report is greater than the Min fanout value
-override_pcf	pcf file on rerun
-enable_timing_commands	Turn OEM commented out constraints back on
-devmap_control_set_num	minimum number of triggers under the same control set . But when the number of flip-flops is less than the threshold, the gating signal is implemented as a data path with LUT . Control set refers to the clock, enable signal, and RST signal of the flip-flop. Optimizing this control signal can increase resource usage
-devmap_const_prop	Mainly used to optimize the constant logic of the input. Constant logic mainly refers to VCC , GND logic. The optimization operation mainly disconnects or optimizes the original VCC and GND

	to the optimal state through the inherent characteristics of the circuit.
-devmap_remove_dups	The main function of this function is to merge some repetitive logic, which belongs to the area optimization option. However, this operation will also affect the copy work in the synthesis stage, which will degrade the timing performance.

Table 9 -9 dev_map

9.10 gen_bit_stream generates a configuration bitstream

options	
-help	print help message
-create_bit_file	Choose whether to generate a bitfile
-create_bin_file	Choose whether to generate a header-less bitfile
-compress_bitstream	Choose whether to compress the bitstream file
-optimize_compress	Choose whether to optimize the compressed bitstream
-write_drm_data	Choose whether to write DRM data
-unused_io_status	the state of unused IO
-usercode	Assign a value to the user identification register, enter an 8 -digit hexadecimal user code , and the value will be written into the bit stream file
-master_configuration_clock_frequency	Master mode clock clk frequency selection
-system_clock_frequency	Configure memory clock mclk frequency selection
-enable_osc_shut_off	Controls whether user logic is allowed to power down the OSC
-enable_watchdog_in_user_mode	Select whether to enable the watchdog in user mode
-enable_watchdog_in_configuration_mode	Select whether to enable the watchdog in configuration mode
-load_watchdog	Set watchdog timeout
-enable_version_select_pin	Enable version control pin
-enable_version_fallback	Choose whether to enable version rollback
-set_fallback_retry_times	Set the number of version rollback attempts
-set_bitstream_retry_times	Set the number of bitstream attempts
-rst_n_pin	Select the pull-down or floating of the RST pin
-enable_external_master_configuration_clock	Select whether to enable the external master configuration clock
-bpi_read_cycle	Select BPI read cycle
-bpi_page_size	Choose the page size for the BPI
-bpi_mode	Select the mode of BPI
-enable_done_synchronization	Select whether the Done signal is synchronized
-wake_up_time_slot_length	Wake-up cycle length selection, namely T1 , T2 , T3 time interval
-done_time_slot	Done signal pulled high time selection
-gwen_time_slot	Gwen signal pulls high time selection
-grsn_time_slot	Grsn signal pull up time selection

-gouten_time_slot	gouten signal is pulled high
-enable_wait_dci_match	Wake up waiting for DCI match
-enable_wait_pll_lock	PLL on wakeup
-wake_up_clock	Choose wake up clock
-create_mask_file	Select whether to generate a mask file to determine the comparison rules between the readback file and the original file.
-persist_slave_parallel_pins	Controls whether the external parallel port is reserved for readback after configuration in parallel mode is complete
-master_configuration_clock_frequency_in_read_back	Readback Clock Selection
-disable_readback_crc	CRC verification on readback
-enable_crc_clock_in_read_back	Enable readback CRC clock
-persist_ipal	Controls whether the internal parallel port is reserved for readback after configuration is complete
-bitstream_security	Control readback configuration memory
-encrypt_bitstream	Choose whether to encrypt the bitstream file
-select_key_type	Configure whether to use internal KEY
-starting_cbc_value	The user manually enters the initial CBC string, the characters are in hexadecimal , and the input length is up to 32 characters
-input_encryption_key_file	select nky file
-key_string	user manually enters the key string, the characters are hexadecimal characters, and the input length is up to 64 characters
-sram_retention	Enable SRAM retention test

Table 9 -10 bit stream

9.11 gen_netlist generates a netlist

options	
-help	print help message
-func_sim_only	Whether to enable only generate sim.v file
-sdf_annotate	sdf file will be called in sim.v , if it is not checked, it will not be called
-process_corner	Decide what type of sdf file to generate

Table 9 -11 Generate netlist

9.12 pnr place and route design

options	
-help	print help message
-dc_duplication	Checked for adaptive insertion and copying of logical units, unchecked for no processing
-plc_decongestion	Set Area Expansion Factor
-gplace_seed	Set random seed value

-gplace_times	Set how many random seeds to run
-seed_step	Set the step size of the seed
-saved_outcome	Sets the number of best seed run results to keep
-parallel	Set the maximum number of concurrently executing seeds
-fast_router	Check to use global routing, uncheck to not use
-fast_router_mode	Set the mode of global routing
-share_router_control_signal	Check to use Control Chain , uncheck to not use
-use_global_ioclkgate	Whether to insert IOCLKGATE
-mode	which pnr operates
-optimize_multi_corner_timing	design should be optimized in all modes to meet timing during the place and route phase
-place_only	Checking means that only the layout is run, and the routing is not run
-fix_hold_violation	Check it to fix hold violations, and uncheck it to not fix it
-fix_hold_violation_iterations	Maximum number of repair hold violations
-fix_hold_violation_threshold	Use this option to perform Hold timing optimization on timing paths with slack less than this value
-fix_hold_violation_in_route	hold violation in the wiring, and uncheck it to not fix it
-fix_hold_violation_threshold_for_clock_path_cross_srb	Use this option to perform Hold timing optimization on timing paths with slack smaller than this value. Only takes effect when the corresponding clock passes through the SRB
-fix_hold_violation_threshold_for_clk_tree	Use this option to perform Hold timing optimization on timing paths with slack smaller than this value. Only takes effect when the corresponding clock does not pass through the SRB
-input_place_db_file	
-refineplacement_cluster	Enable packing switch during detailed layout
-refineplacement_iteration	Detailed Layout Convergence Properties
-plc_initial_method	Global layout initialization starting position
-early_block_placement	Enable Macro Instance priority placement switch
-auto_dispose_macro	PDS software self-adaptive selection macro module priority placement switch
-dispose_drm_prior	When the user chooses to disable the PDS software to adaptively select the macro module to be placed first, the user chooses the placement order of the DRM
-dispose_apm_prior	When the user chooses to disable the PDS software to adaptively select the macro module to be placed first, the user chooses the placement order of the APM
-dispose_dram_prior	When the user chooses to disable the PDS software to adaptively select the macro module to be placed first, the user selects the placement order of the DRAM
-dispose_carrychain_prior	When the user chooses to prohibit the PDS software from adaptively selecting the priority placement of macro modules, the user independently selects the placement order of the Carry Chain
-slack_prior_in_global_router	Global winding Slack priority mode
-slack_weight	Controlling the Weight of Timing Factors in the Routing Process

-pin_cost_increasing_speed	Increased cost of congested Pins
-congest_overlap_limit	Control the maximum number of routing iterations in congestion routing mode
-max_ctrl_chain_length	CE/RS control signal chain maximum length

Table 9 -12 pnr

9.13 report_power reports power consumption information

options	
-help	print help message
-tempgrade	temperature class
-process	process deviation
-custom_junction	Whether the user specifies the node temperature
-ambient	ambient temperature
-junction	Specify nodal temperature
-custom_ja	User Specified Thermal Coefficient
-theta_ja	Specify thermal coefficient
- ariflow	airflow conditions
-heat sink	Heat dissipation
-theta_sa	Heat dissipation thermal resistance coefficient
-board_thermal	Board heat dissipation
-output_ppr	Power Consumption Report Output File
-output_pps	Project Power Reporting Settings File
-output_ppf	Power consumption evaluation file exported to PPP
-vcd	The user-specified post-simulation file, which records the simulation waveform, through which the signal reversal can be obtained
-tb_module	module name in the simulation file specified by the user
-design_name	The instantiated name of the user-specified design design in the test bench
-output_pf	IO external load
-clk_freq	default clock frequency
-togg	Default flip rate
-prob	Default static high level probability
-io_togg	Default toggle rate for I/O
-io_prob	Default enable probability of I/O
-ram_togg	Default flip rate for DRM
-ram_prob	The default enable probability of DRM
-dsp_togg	Default flip rate for APM
-dsp_prob	The default enable probability of APM
-hsst_togg	Default rollover rate for HSST
-hsst_prob	The default enable probability of HSST

-vcc	VCC voltage
-vccio33	Bank VCCIO3.3 voltage
-vccio25	Bank VCCIO2.5 voltage
-vccio18	Bank VCCIO1.8 voltage
-vccio15	Bank VCCIO1.5 voltage
-vccio12	Bank VCCIO1.2 voltage
-vccaux	Auxiliary power supply VCCAUX voltage
-vcc33a	VCCAUX.Default voltage
-vccint	VCC.Default voltage
-vcc33	VCCAUX.Default voltage

Table 9 -13 report power

9.14 report_timing reports timing information

options	
-help	print help message
-delay_type	Set the type of timing analysis
-nworst	Sets the maximum number of paths reported by each timing path endpoint
-max_path	Set the maximum number of paths for timing reports
-input_pins	Show Input Pins
-slack_greater_than	Set the reported slack minimum scope
-slack_less_than	Set the slack maximum scope for reporting
-disable_package_delay	Set whether the timing report calculates the delay of the package (package pin)
-report_io_datasheet	Set whether the timing report reports the timing characteristics of IO
-ignore_db_version	Do not check DB version
-from	from node of the timing path in the timing report
-to	to node of the timing path in the timing report
-through	through node of the timing path in the timing report

Table 9 -14 report_timing

9.15 compile_simlib compiles the simulation library

Options	
-help	print help message
-Simulator	Emulator to use when compiling the library
-family	Specify the chip series to compile the simulation library
-language	Specifies the hardware description language type
-library	Specify the type of compiled emulation library

-simulator_exec_path	The path where the emulator executable file is located
-directory	Specifies the folder where the compiled simulation library is saved

Table 9 -15 Simulation

10 Common errors

10.1 Constraint error

Error number	Error description	Solution
Constraint Editor 0008		
Constraint Editor 0009		
Constraint Editor 0010		
Constraint Editor 0011		
Constraint Editor 0012		
Constraint Editor 0013		
Constraint Editor 0014		
Constraint Editor 0015	In the constraint command def_port , the keyword specifying the constraint to a certain location must be LOC	
Constraint Editor 0047		
Constraint Editor 0048		
Constraint Editor 0049		
Constraint Editor 0050		
Constraint Editor 0051		
Constraint Editor 0052		
Constraint Editor 0053		
Constraint Editor 0054		
Constraint Editor 0055		
Constraint Editor 0056		
Constraint Editor 0057		
Constraint Editor 0058		
Constraint Editor 0059		
Constraint Editor 0060		
Constraint Editor 0061		
Constraint Editor 0062		
Constraint Editor 0063		

Table 10 -1 constraint error

10.2 Physical Constraint Editor

Error number	Error description	Solution
PhysicalConstraintEditor 0001	The given coordinates are not within the coordinate range set by the model	

PhysicalConstraintEditor 0002	The given cell is illegal or has no corresponding implementation	
PhysicalConstraintEditor 0003	The specified device instance was not found	
PhysicalConstraintEditor 0004	The given resource file does not exist or failed to load	
PhysicalConstraintEditor 0005	The given package pin is invalid	
PhysicalConstraintEditor 0006		
PhysicalConstraintEditor 0007		
PhysicalConstraintEditor 0016	The specified instance is not a logic instance	
PhysicalConstraintEditor 0017	Constrain the same object multiple times	
PhysicalConstraintEditor 0018	The constraint format is incorrect, no value is specified for the keyword	
PhysicalConstraintEditor 0019		
PhysicalConstraintEditor 0020		
PhysicalConstraintEditor 0021		
PhysicalConstraintEditor 0022		
PhysicalConstraintEditor 0023		
PhysicalConstraintEditor 0024	A specific area must be specified, represented by two coordinates (x1,x2,y1,y2)	
PhysicalConstraintEditor 0025		
PhysicalConstraintEditor 0026		
PhysicalConstraintEditor 0027		
PhysicalConstraintEditor 0028		
PhysicalConstraintEditor 0029		
PhysicalConstraintEditor 0030		
PhysicalConstraintEditor 0031		
PhysicalConstraintEditor 0032		
PhysicalConstraintEditor 0033		
PhysicalConstraintEditor 0034	region name must be composed of strings, numbers, and underscores, and cannot start with a number	
PhysicalConstraintEditor 0035	region must be in the form of two coordinates (x1,x2,y1,y2)	
PhysicalConstraintEditor 0036	Specifies that the object is defined repeatedly without passing through the region	
PhysicalConstraintEditor 0037		
PhysicalConstraintEditor 0038		
PhysicalConstraintEditor 0039		
PhysicalConstraintEditor 0040		
PhysicalConstraintEditor 0041		

PhysicalConstraintEditor 0042		
PhysicalConstraintEditor 0043		
PhysicalConstraintEditor 0044		
PhysicalConstraintEditor 0045		
PhysicalConstraintEditor 0046		

Table 10 -2 PCE error

10.3 UserConstraintEditor

Error number	Error description	Solution
UserConstraintEditor 0001	The configuration item that the current configuration item depends on is missing	
UserConstraintEditor 0002	An unsupported option was specified	
UserConstraintEditor 0003		
UserConstraintEditor 0004	command: %s not support!	
UserConstraintEditor 0005		
UserConstraintEditor 0006	No corresponding value is specified for the specified option	
UserConstraintEditor 0007	The correct command line format was not given	
UserConstraintEditor 0008	The specified object is invalid	
UserConstraintEditor 0009	Incorrect constraint command specified	
UserConstraintEditor 0010	Objects that must be specified are not defined	
UserConstraintEditor 0011		
UserConstraintEditor 0012	The type of the specified object is not given to distinguish	
UserConstraintEditor 0013		
UserConstraintEditor 0014		
UserConstraintEditor 0015		
UserConstraintEditor 0016		
UserConstraintEditor 0017		

Table 10 -3 UCE error

10.4 Flow error

10.4.1 FabFlow

Error number	Error description	Solution
FabFlow 0001	Prompt that no design file has been added	Double-click or right-click Designs in Pango Design Suite->Navigator to add design files
FabFlow 0002	The file does not exist or the file failed to open	

FabFlow 0003	The current action does not define the corresponding CanbeRun processing function	Check the calling behavior of the action to determine whether it is correct, and reimplement the CanbeRun function of the action if necessary
FabFlow 0004	The current action executes a function that has not been overridden	Check the calling behavior of the action to determine whether it is correct, and reimplement the specific function of the action if necessary
FabFlow 0005	The current action executes an executor function that has not been rewritten	Check whether the calling behavior of the action is correct, and reimplement the executor function of the action if necessary
FabFlow 0006	arch load , usually accompanied by other detailed error messages	Locate the problem based on detailed information
FabFlow 0007	Detected that there is currently no Design file	Double-click or right-click Designs in Pango Design Suite->Navigator to add design files
FabFlow 0008	Synthesis tool does not set path	menu bar : Tools -> Preference -> Set the path of Synplify pro
FabFlow 0009	fails to call Synplify synthesis	
FabFlow 0010	synplify_impl folder generated by Synplify after the integrated version synthesis	Find the folder and delete it manually
FabFlow 0011	design is returned after reading the DB during Flow execution	
FabFlow 0012	An empty string is passed in when Flow reads the DB	
FabFlow 0013	Failed to read DB	
FabFlow 0014	DB file does not match the currently executed Action	
FabFlow 0015		
FabFlow 0016	Single-step execution of action and normal execution of action cannot be performed at the same time	Execute the clean -all command
FabFlow 0017	Failed to write DB file	
FabFlow 0018	Failed to update Action state	
FabFlow 0019	The current software does not support the project file	
FabFlow 0020	Failed to read design name from DB	
FabFlow 0021	Timing library failed to load	
FabFlow 0022		
FabFlow 0023		
FabFlow 0024		
FabFlow 0025		
FabFlow 0026		
FabFlow 0027		
FabFlow 0028	Chip device model is not set	source page Icons set chip device signal
FabFlow 0029	Synplify does not set OEM device type	source page icon set
FabFlow 0030	Multiple design files contain the same module name, and the module is set as the top module	Delete the file containing the module with the same name in design
FabFlow 0031	Synthesis failed or file does not have read and write permissions	rerun synthesis
FabFlow 0032	file pointer is null	
FabFlow 0033		

FabFlow 0034		
FabFlow 0035	Failed to convert attributes to physical constraints file	
FabFlow 0036		
FabFlow 0037		
FabFlow 0038		
FabFlow 0039		
FabFlow 0040		
FabFlow 0041		
FabFlow 0042		
FabFlow 0043		
FabFlow 0044		
FabFlow 0045		
FabFlow 0046		
FabFlow 0047		
FabFlow 0048		
FabFlow 0049		
FabFlow 0050		

Table 10-4 FabFlow

10.4.2 DB

Error number	Error description	Solution
DB 0001		
DB 0002		
DB 0003		
DB 0004		
DB 0005		
DB 0006		
DB 0007		
DB 0008		
DB 0009		
DB 0010		
DB 0011		
DB 0012		
DB 0013		
DB 0014		
DB 0015		
DB 0016		
DB 0017		
DB 0018		

DB 0019		
DB 0020		
DB 0021		
DB 0022		
DB 0023		
DB 0024		
DB 0025		
DB 0026		
DB 0027		
DB 0028		
DB 0029		
DB 0030		
DB 0031		
DB 0032		
DB 0033		
DB 0034		
DB 0035	An Error Occurs When Reading and Writing to the DB During Flow Running	In general, this kind of problem cannot be solved, you can try to re-run Flow to generate a new DB file
DB 0036		
DB 0037		
DB 0038		
DB 0039		
DB 0040		
DB 0041		
DB 0042		
DB 0043		
DB 0044		
DB 0045		
DB 0046		
DB 0047		

Table 10-5 DB

10.4.3 wxya

Error number	Error description	Solution
UiWgt 0001	to get FAB_CFG_PATH path	Add FAB_CFG_PATH environment variable
UiWgt 0002	Fab software is forward compatible, and the old version of the Fab software is not compatible with the new version of the Fab project file	Upgrade Fab software

UiWgt 0003	No permission to read and write the project file or the project file is already occupied by other processes	
UiWgt 0004	The integrated version fails to call the synthesis tool for synthesis	
UiWgt 0005	option already exists in the action	
UiWgt 0006		
UiWgt 0007	The plug-in failed to execute the operation. For specific reasons, please refer to the prompt information of the plug-in called	
UiWgt 0008	Fab software cannot find the plugin	Reinstall the fab suite
UiWgt 0009	Failed to call plugin	
UiWgt 0010		
UiWgt 0011		

Table 10-6 UiWgt

10.5 DRC error

Error number	Error description	Solution
DRC 0001	IO inst in the user design netlist . It may be that the relevant inst was not inserted during synthesis	Modify the settings in the synthesis related options
DRC 0002	Design designed by the user , the Port is connected to multiple IO inst	Modify Design Use Case
DRC 0003	Due to the limitations of the chip architecture, some ports cannot be directly connected to the chip ports, and the design uses direct connections. This problem typically occurs when instantiating GTP units directly. If GTP_LUTADDSUB is used as the first level, its CIN port must be suspended	Modify the settings in the synthesis related options
DRC 0004	Design designed by the user , some inst Pins must be connected to GTP_LUT5CARRY	Insert GTP_LUT5CARRY in these intermediate stages
DRC 0005	Due to the limitations of the chip architecture, some GTP_LUT5CARRY and GTP_LUTADDSUB ports COUT cannot be directly connected to ports other than CIN , and the design uses a direct connection. This problem typically occurs when instantiating GTP units directly. If GTP_LUTADDSUB is used as an intermediate stage, its CIN port must only be connected to the COUT of GTP_LUT5CARRY or GTP_LUTADDSUB	Insert GTP_LUT5CARRY or GTP_LUTADDSUB in these intermediate stages , so that the COUT of this stage is output from the COUT and SUM ports of the inserted stage at the same time
DRC 0006	Due to the limitations of the chip architecture, some Insts cannot be directly connected to ports other than CIN , and the design uses direct connections. This problem typically occurs when instantiating GTP units directly.	Insert GTP_LUT5CARRY or GTP_LUTADDSUB in these intermediate stages , so that the COUT of this stage is output from the COUT and SUM ports of the inserted stage at the same time
DRC 0007	Due to the limitations of the chip architecture, some Insts cannot be directly connected to ports other than CIN , and the design uses direct connections. This problem typically occurs when instantiating GTP units directly. For example , port I0 of GTP_MUX2LUT7 must be connected to port Z of GTP_MUX2LUT6	Follow the prompts to insert the corresponding GTP
DRC 0008	Due to the limitations of the chip architecture, there are fixed connections between some GTPs	Follow the prompts to modify the corresponding GTP connection

	. This problem typically occurs when instantiating GTP units directly. For example , GTP_CLKDELAY must be connected to GTP_INBUFG	
DRC 0009	Due to the limitations of the chip architecture, there are fixed connections between some GTPs . This problem typically occurs when instantiating GTP units directly. For example , the port "IFIFO_RADDR[0]" of GTP_DLL must be connected to GTP_DDC	Follow the prompts to modify the corresponding GTP connection
DRC 0010	Due to the limitations of the chip architecture, there are fixed connections between some GTPs . This problem typically occurs when instantiating GTP units directly. For example , the port "PADT" of GTP_OGDDR and GTP_DDC must be connected, and cannot be connected with other inst	Follow the prompts to modify the corresponding GTP connection
DRC 0011	The main reason for this problem is that there are units that cannot be Packed, such as GTP_IODELAY and GTP_IBUF must be directly connected, if the rules are not met, Packing will fail	Follow the prompts to modify the corresponding GTP connection
DRC 0012	The main reason for this problem is that there are units that cannot be packed in DDR , such as GTP_IGDES7 and GTP_IBUF are not connected correctly. If the rules are not met, Packing will fail.	Follow the prompts to modify the corresponding GTP connection
DRC 0013	The main reason for this problem is the internal problem of the software . When the port DESCLK on the DDR is connected to the SAMPLE_CLK or PROBE_CLK of the DCC , the parameter DESCLK_SRC needs to be modified accordingly.	Follow the prompts to modify the corresponding GTP connection
DRC 0014	The main reason for this problem is the internal problem of the software . When the port DESCLK on the DDR is connected to the SAMPLE_CLK or PROBE_CLK of the DCC , the parameter DESCLK_SRC needs to be modified accordingly.	
DRC 0015	The main reason for this problem is wrong user constraints. Like the two IOs in a Bank , the standard setting is LVCMOS33 , LVCMOS15 or conflicting reference voltage options are set	Check IO standard settings
DRC 0016	Design or corresponding pcf file designed by the user , unsupported IO standard attributes are set in some Banks	Check IO standard settings
DRC 0017	During software processing, GTP resources that cannot be laid out appear	Check User Design
DRC 0018	The resources of the user design after synthesis exceed the resources that the chip can provide	Modify the design use case or change to another chip
DRC 0019	Design or corresponding pcf file designed by the user , an unsupported IO standard attribute is set	Check IO standard settings
DRC 0020	pcf file added by the user , two IOs in the same IO Group must set the same standard	Modify the corresponding IO standard
DRC 0021		
DRC 0022		
DRC 0023		
DRC 0024		
DRC 0025		
DRC 0026		
DRC 0027		

DRC 0028		
DRC 0029		
DRC 0030		
DRC 0031		

Table 10 -7 DRC error

10.6 map

Error number	Error description	Solution
DeviceMap 0001	According to the Fab software model, some Inst must exist in the form of Group	
DeviceMap 0002	the user-designed Design , when the GTP unit is instantiated, the connection relationship between them is wrong	Follow the prompts to modify the corresponding GTP connection
DeviceMap 0003	The main reason for this problem is that there are units that cannot be Packed, such as GTP_IODELAY and GTP_IBUF connection errors	Follow the prompts to modify the corresponding GTP connection
DeviceMap 0004	STARTs in the user design exceeds the number allowed by the chip	Modify Design Use Case
DeviceMap 0005	GRS in the user design exceeds the number allowed by the chip	Modify Design Use Case
DeviceMap 0006		
DeviceMap 0007		
DeviceMap 0008		
DeviceMap 0009		

Table 10 -8 maps

10.7 PLACE

Error number	Error description	Solution
Place 0001	Cells participating in layout or constraints must be Log Inst	
Place 0002	User design resources exceed the number allowed by the chip	Modify test cases to reduce resources or choose other chips
Place 0003	User design resources exceed the number allowed by the chip	Modify test cases to reduce resources or choose other chips
Place 0004	The IO ports that users connect to DQS must be bound in the same DQS group	Modify constraints file
Place 0005	Through the layout algorithm, the Inst layout fails . There are many reasons for this, usually the following reasons: 1. Critical resource situation. 2. Constraint errors	Provide constraint information to help the software layout more reasonably
Place 0006	Through the layout algorithm, the Inst layout fails . There are many reasons for this, usually the following reasons: 1. Critical resource situation. 2. Constraint errors	Provide constraint information to help the software layout more reasonably
Place 0007	DLL and DQS constraints conflict, if you press this constraint, it will lead to unsuccessful wiring	Provide constraint information to help the software layout more reasonably

Place 0008	DLL and DQS constraints conflict, if you press this constraint, it will lead to unsuccessful wiring	Provide constraint information to help the software layout more reasonably
Place 0009	Due to chip architecture issues, a single USCM can only drive a quarter quadrant. When the software is processing, it copies the units into four parts. If one of them is constrained, other USCM units must be constrained	the USCM backup unit
Place 0010	Wrong USCM number, resulting in a USCM name mismatch	
Place 0011	Due to chip architecture issues, a single USCM can only drive a quarter quadrant. When the software is processing, it copies the units into four parts. If one of them is constrained, other USCM units must be constrained	the USCM backup unit
Place 0012	In the user design, GTP_CLKBUFG , GTP_CLKBUFGCE and other GTPs that require USCM resources are too many	Modify the design use case and reduce the relevant GTP
Place 0013	The user-constrained IO standard is not supported in this device or the standard name is wrong	Check standard names in pcf
Place 0014	of IOB and IOL in IO Group is wrong	
Place 0015	IOB does not exist in IO Group	
Place 0016		
Place 0017	In the FAB software, the Group could not find a suitable position	Guide layout with manual constraints
Place 0018	IO standard property of the user constraint is wrong	check constraints file
Place 0019	IO standard attribute of the user constraint is wrong. If different VCCIO standards are set in the same Bank	check constraints file
Place 0020	User constraint error. When setting a standard attribute with a reference voltage, the corresponding IO used to set the reference voltage can not constrain the IO port	check constraints file
Place 0021	Ref Pin layout failed. When setting a standard attribute with a reference voltage, the corresponding IO used to set the reference voltage can not constrain the IO port	check constraints file
Place 0022		
Place 0023	The VCC/GND model is wrong, and the corresponding implementation method is not supported	Replace other series
Place 0024	The model is wrong, and the corresponding implementation method is not supported	Replace other series
Place 0025	There are no layoutable resources at the location corresponding to the Floor Plan	Replace other series
Place 0026	The model is wrong, and the corresponding implementation method is not supported	Replace other series
Place 0027	When laying out, inst is arranged outside the chip , user constraint error or software error!	Modify User Constraints
Place 0028	layout results, the layout of each Inst in the Group fails	
Place 0029		
Place 0030	According to the software model, some units have multiple implementations according to different resources. The problem is that the wrong implementation	check constraints file

	is used in the constraints process. For example, on CLMA , GTP_LUT uses the CLMS implementation	
Place 0031	The model is wrong, and the corresponding implementation method is not supported	Replace other series
Place 0032	The model is wrong, and the corresponding implementation method is not supported	Replace other series
Place 0033	Software model error. The port on the Time model is found on the instance	Replace other series
Place 0034	GTP unit is instantiated directly , and the connection between these GTP units is wrong. For example , the CLKIN port of GTP_CLKDELAY can only be connected with GTP_INBUFG or GTP_INBUFGDS	modify user design
Place 0035	CLK_DELAY conflicts with connected CLK PAD constraints	Check user constraints file
Place 0036	On the current chip, the number of CLK PADs is not enough, resulting in layout failure	
Place 0037	CLK PAD resources are insufficient, or the connected Inst constraints are wrong	Modify constraints file
Place 0038	CLK PAD resources are insufficient, or the connected Inst constraints are wrong	Modify constraints file
Place 0039	Insufficient device resources	Modify the design use case or replace other devices
Place 0040		
Place 0041		
Place 0042		
Place 0043		
Place 0044		
Place 0045		
Place 0046		
Place 0047		
Place 0048		
Place 0049		
Place 0050		
Place 0051		
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Place 0068		
Place 0069		
Place 0070		
Place 0071		
Place 0072		
Place 0073		
Place 0074		
Place 0075		
Place 0076		
Place 0077		

Table 10-9 place

10.8 Route error

Error number	Error description	Solution
Route 0001	detected in the net , that is, there is no wiring path between the start and end points.	
Route 0002	It was detected in the routing module that the current state is not routing.	
Route 0003	detected in a net . A net is only allowed to have one driver.	
Route 0004	loading wiring result stage of manual wiring , an exception was found	
Route 0005	Failed to find an arc in a certain mux .	
Route 0006	Put VCC , GND and other applications on a certain circuit unit, but no suitable circuit can be found.	
Route 0007	A load needs to be rewired, but the corresponding wiring pin is not found .	
Route 0008	Wiring failed.	
Route 0009		
Route 0010		
Route 0011		
Route 0012		
Route 0013		
Route 0014		
Route 0015		
Route 0016		
Route 0017		

Table 10 -10 router

10.9 Design Editor error

Error number	Error description	Solution
DesignEditor 0001	Routing Arc is used for wiring , the corresponding Design Net cannot be found through the Src port .	
DesignEditor 0002	After the wiring is completed, there is still a Design Net without a driver, and a Design Net must have a driver .	
DesignEditor 0003	When drawing a line, the anchor passed by the current Design Net is empty.	
DesignEditor 0004	PnR , loading the PnR DB file fails.	
DesignEditor 0005	PnR , its DB file is not imported.	

Table 10 -11 DE error

10.10 Timing error

Error number	Error description	Solution
Timing 0001	After the PnR is completed , there is still no mapping from the design port to the arch pin , because in the user design, each design port must be connected to an IO buffer component.	
Timing 0002	design net to arch pin failed	
Timing 0003	When the design port type is INOUT , when the connection relationship between the nodes at both ends of the port cannot be saved, an error will be reported.	
Timing 0004	When instantiating a grid device , an Instance with internal logic cannot be created, which will result in the failure to create a sequence diagram of the device .	
Timing 0005	Failed to construct sequence diagram for routing network	
Timing 0006	When creating the timing path in the arch , the delay value connected to it cannot be obtained , resulting in this error.	
Timing 0007	The grid device does not obtain the timing view from the base device view , so the timing netlist cannot be constructed.	
Timing 0008	There are two reasons: the first is that when the timing graph is copied to the top -level architecture , the app node is not directly connected to the IT node ; the second is that the construction of the timing table is canceled midway.	
Timing 0009	In the timing diagram, the delay is saved in the timing view , the type is port , and the timing view has been deleted before the delay is transferred to the timing diagram	
Timing 0010	1. The timing diagram was not obtained from the timing table, which caused this error; 2. The timing node was not found in the timing diagram .	
Timing 0011	Some files are missing, and the specific situation should be analyzed according to the error message.	

Timing 0012	It may be that the src port , snk port and arc in the routing arc are not found, check these ports in the file .	
Timing 0013	The Instancce of the device has not been obtained .	
Timing 0014	delay model is not supported in the hardware model .	
Timing 0015	This device was not found in the arch	
Timing 0016	timing node was not found or failed to be created, resulting in failure to mark the timing info in the timing table .	
Timing 0017		
Timing 0018	Timing node name error	
Timing 0019	grid device has multiple input drivers	
Timing 0020	timing arc defined in the ctf file was not found in the tm file	Modify the tm file or ctf file
Timing 0021	D pin in the latch must be connected to the starting of the delay arc , otherwise an error will be reported.	
Timing 0022	D pin in the latch must be connected to the ending of the check arc , otherwise an error will be reported.	
Timing 0023	instance has already been created, an error will be reported if it is created again.	
Timing 0024	Port not found in timing cell	
Timing 0025	This unit has not been added to the library and is currently not supported.	
Timing 0026	The corresponding prim device was not found in the device	
Timing 0027	corresponding pin was not found in the device	
Timing 0028	timing model was not found in vop	
Timing 0029	More than one instance is placed on the grid device .	
Timing 0030	mapping the pins in the structure netlist to the timing netlist , the corresponding pin is not found in the timing netlist .	
Timing 0031		
Timing 0032		
Timing 0033		
Timing 0034	timing view was not found in the grid device	
Timing 0035	delay model was not found in the grid device	
Timing 0036	In the layout, a pin has multiple drive inputs or accepts multiple signals, which makes it impossible to build a timing diagram.	
Timing 0037	The Istance instantiated in the base netlist is not obtained , resulting in the inability to map .	
Timing 0038	Design is not flattened. Sequence diagram construction failed	
Timing 0039	Failed to construct the timing netlist, the timing diagram endpoint was not found in the drive pin	
Timing 0040	Failed to construct timing diagram, timing netlist endpoint not found in accept pin	
Timing 0041	For clock transmission, the clock edge type must be 01 or 10 , XX is not allowed .	
Timing 0042	Some functions are not implemented in the current version.	
Timing 0043	domain already exists, no more domain can be added	

Timing 0044	The above type is not supported in the template category.	
Timing 0045	The above type is not supported in the template category.	
Timing 0046	The above type is not supported in the template category.	
Timing 0047	The above type is not supported in the template category.	
Timing 0048	The above type is not supported in the template category.	
Timing 0049	The above type is not supported in the template category.	
Timing 0050	The above type is not supported in the template category.	
Timing 0051	The above type is not supported in the template category.	
Timing 0052	The above type is not supported in the template category.	
Timing 0053	The above type is not supported in the template category.	
Timing 0054	The above type is not supported in the template category.	
Timing 0055	The above type is not supported in the template category.	
Timing 0056	The above type is not supported in the template category.	
Timing 0057	The above type is not supported in the template category.	
Timing 0058	The above type is not supported in the template category.	
Timing 0059	Generally, it is a name conflict, modify the name of the library file.	
Timing 0060	The corresponding template has been declared	
Timing 0061	The corresponding unit has declared	
Timing 0062	Cannot add port bus, the port bus already exists	
Timing 0063	Cannot add port, port already exists	
Timing 0064	in the command \"set_clock_latency\" is not a clock pin	
Timing 0065	Unable to determine the trigger edge of launch clock and capture clock	
Timing 0066	unknown mistake	
Timing 0067	\'set_input_delay\' failed, the corresponding port was not found in the sequence diagram	Modify the port to be set
Timing 0068	\'set_output_delay\' failed, the corresponding port was not found in the sequence diagram	Modify the port to be set
Timing 0069	The initial data cannot be saved	
Timing 0070	calculation fails somewhere in the entire timing propagation , and the analysis starts from the beginning along the timing propagation .	
Timing 0071	Unable to determine the relationship between launch clock and capture clock	
Timing 0072	clock already exists	
Timing 0073	clock group already exists	
Timing 0074	Timing calculations are performed at the Top-level , and netlist cannot construct timing diagrams.	
Timing 0075	Combinational loop found in line, timing analysis failed	Check the circuit, remove the loop
Timing 0076	Failed to create timing diagram, same as timing 0074	

Timing 0077	Clocks for unknown signal transitions cannot be transmitted	Redefine the clock signal
Timing 0078	Timing model library not found	
Timing 0079	Physical timing model library not found	
Timing 0080	Physical timing model library not found	
Timing 0081	Physical timing model library not found	
Timing 0082		
Timing 0083		
Timing 0084		
Timing 0085		
Timing 0086		
Timing 0087		
Timing 0088		
Timing 0089		
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Timing 0155		
Timing 0156		
Timing 0157		
Timing 0158		
Timing 0159		

Table 10 -12 timing error

10.11 Simulation error

Error number	Error description	Solution
Simulation 0006	The executable file for the emulator could not be found at the specified path	Specify the path as under the folder with the emulator executable
Simulation 0007	This type of emulator is not supported	The simulators currently supported by the software include Modelsim and Questasim , just choose one of them
Simulation 0008	The compiled simulation library does not exist	Run the compiled simulation library first, where the family option should be consistent with the chip series when running the simulation

Table 10 -13 Simulation error

11. Contacts

Контакты для технических и коммерческих вопросов

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